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### 論文内容の要旨

In this dissertation, the author would like to present a novel method for reducing energy dissipation utilizing a two-phase clocked adiabatic static CMOS logic (2PASCL) topology. The word “adiabatic” (Greek *adiabatos*, which means impassable) indicates a state change that occurs without heat loss or gain. Simulation results show that the power dissipation of 2PASCL multipliers is about 55% less than CMOS multipliers for both 0.18  $\mu$ m and 1.2  $\mu$ m CMOS processes. 4×4-bit array 2PASCL multiplier is fabricated and its functionality is verified. 2PASCL is easily derived from CMOS topology. During adiabatic switching, all the nodes are charged or discharged at a constant current in order to minimize power dissipation. Moreover, it uses a two-phase clocking split-level sinusoidal power supply, wherein  $V_{\phi}$  and  $V_{\phi}$  to replace  $V_{dd}$  and  $V_{ss}$ , respectively. From the analytical study, during adiabatic charging, when the time for the driving voltage to change from GND to  $V_{dd}$ ,  $\tau$  is long, power dissipation is nearly zero. Energy recovery is also demonstrated.

In Chapter 1, author starts with the history and major milestone that leading to the development of nowadays processors. The author also mentions about the importance of reducing the power dissipation as the circuits becoming denser and faster. Low-power techniques currently implemented in device and circuit levels are also given. Finally, a brief introduction of adiabatic technology, its condition and requirements are emphasized. The requirements are — voltages between current-carrying electrodes must be zero when the transistors switch to the on state and the conductive coupling between the capacitor  $C$  and the driver must exist at any time. AC power supplies are utilized to initially charge the circuit during specific adiabatic phases and then discharge the circuit to recover the supplied charge.

In Chapter 2, analytical analysis of CMOS and adiabatic circuit is performed. Both pMOS and nMOS transistors can be modeled by including a resistor in order to represent the effective channel resistance of the switch and the interconnect resistance. Then simulation results using LTspice with 0.18  $\mu$ m CMOS technology were carried out on the conventional adiabatic inverter logic circuits to verify their logic functionality and compare the power dissipation. Finally, the effect of the load capacitance in the adiabatic circuits is also investigated.

Chapter 3 introduces two-phase clocked adiabatic static CMOS logic (2PASCL). Its design has no diodes at the charging path. Thus, the 2PASCL circuit is different from other diode-based adiabatic circuits, in which current flows through the diode and the transistor. In this case, during charging, current flows only through the transistor. With the aforementioned 2PASCL circuit, we can achieve high amplitude and reduce energy dissipation. 2PASCL uses two-diodes; one diode is placed between the output node and power clock, and the other diode is placed adjacent to the nMOS logic circuit and connected to another power source. From the simulation results on the supplied energy, we have confirmed that energy is distributed back to the power sources. Theoretically, these diodes are used to transfer back charges to the power sources from the load capacitor. In energy-recovery circuits, based on the energy conservation law— energy dissipated is equal to the total energy injected to the circuit and the energy received back from the circuit capacitance. In this Chapter, author also concentrates on analysis using simulation results of the proposed 2PASCL circuit for its current values, voltage and energy dissipation. A comparative study of the main distributor for the dissipation energy is also reviewed. Equivalent circuit for 2PASCL inverter is also shown. Then, a details study on the power supply clocks has been done. A power dissipation comparison of triangle, trapezoidal and sinusoidal waveforms is demonstrated. Then, the optimum relationship between power supply clocks and input

signal clocks, separated and overlapped shapes, symmetrical and unsymmetrical shapes were also examined prior to the decision of selecting split-level sinusoidal voltage clocks. Finally 2PASCL fundamental logic family is exhibited.

Chapter 4 is devoted to the design of the application circuits of 2PASCL. To verify the practical applicability of the proposed 2PASCL circuit, a 4-bit 2PASCL Ripple Carry Adder (RCA) was designed and simulated. It is depicted that 2PASCL RCA dissipated only 35% of power compared to CMOS RCA. Then,  $4 \times 4$ -bit array multiplier which consists of sixteen ANDs, 6 full adders and 4 half adders logics is designed and simulated. However, from simulation results of  $0.18 \mu\text{m}$  process,  $4 \times 4$ -bit array 2PASCL multiplier only shows a good logic functionality of up to 200 MHz transition frequency. Author observes some signal degradations for transition frequency of more than 200 MHz. This is due to the charging time  $\tau$  which is much slower than conventional CMOS.  $\tau$  is also proportional to  $RC_L$  i.e. the longer the path, the larger  $\tau$  is needed.

In Chapter 5, the LSI implementation of 2PASCL is elaborated. It includes the layout designs of 2PASCL logics, half-adder, full-adder and D-flip-flops. For 2PASCL LSI implementation,  $1.2 \mu\text{m}$  CMOS technology is utilized. For the fabricated chip, author includes  $4 \times 4$ -bit array 2PASCL multiplier with output signals terminal with and without D-flip-flops. D-flip-flop is implemented to synchronize the output at the same time improve the logic swings and reduce glitches. From the measurement results, the chip is functioning up to 10 MHz input frequency. The actual measurement of power dissipation of the chip from 50 kHz to 5 MHz shows that an average of only 23% of power dissipated compared to CMOS. Finally, the conclusions are drawn in Chapter 6.

### 論文審査結果の要旨

本研究は、2 相の交流電源で駆動する静的断熱 CMOS 論理回路(2PASCL)を提案し、その詳細な消費電力解析を行って最適な動作条件を見出すと共に、基本論理回路やそれらを組み合わせた加算器や乗算器への応用を系統的に検討したもので、学術的に新規性のある多くの知見を得ている。また、LSI を設計試作して実証実験を行い、提案回路および消費電力解析の有効性を確かめており、基礎と応用の両面において断熱原理の基づくこれまでの論理回路設計研究を著しく発展させたものである。

本研究の主な成果は以下の通りである。

- ・論理回路の基本回路となる断熱動作 CMOS インバータを新しく提案している。提案回路の特徴は、ダイオード動作する素子を含ませることで、断熱動作をより効率的なものにしていることにある。その消費電力が最小となる条件を見出すために、ダイオード動作する素子を含む場合の論理回路の断熱動作を記述できるモデルを新しく導出している。そして、このモデルから提案回路の断熱動作の詳細な解析を行い、消費電力最小となる電源波形と素子のパラメータ値を決定している。この方法は、他の断熱回路にも応用できる一般的なものである。

- ・インバータを発展させ、同じ断熱原理に基づく基本論理回路として、NOR, NAND, XOR を提案して、全加算器や D-フリップフロップを始めとする応用回路の設計を可能にしている。特に XOR については、素子数の少ない低消費電力なものになっている。

- ・ $1.2 \mu\text{m}$  スタンダード CMOS 技術を用いて  $4 \times 4$  bit アレイ乗算器を LSI で設計し、従来の CMOS 技術を用いる場合に比較して最大 77% の消費電力が削減可能であることを示している。

- ・上記設計に基づき、 $4 \times 4$  bit アレイ乗算器を試作し、断熱動作する従来の同仕様の乗算器に比較して 57% の消費電力削減を実証している。

### 最終試験結果の要旨

論文提出者は、在学中の 3 年間に於いて、勉学・研究活動に精勤し、所定の講義の単位を取得するとともに、学位申請論文としての研究内容を 2 編の学術論文と 9 編の国際会議論文として公表した。

これらの結果を確認して、学位認定に伴う最終試験の結果を合格と判定する。