別紙様式第１７号

学位論文全文に代わる要約
Extended Summary in Lieu of the Full Text of a Doctoral Thesis

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学位論文題目：
Thesis Title　Non-floating Two-Phase Clock Adiabatic Logic Circuit: Analysis and Application
(フローティング構造を有しない2相クロック断熱的論理回路の解析と応用)

学位論文要約：
Summary of Thesis

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The study concentrates adiabatic inverters which is the one of the basic components of LSI system. We propose a new inverter that improves former inverter with low power consumption. The thesis embraces two themes. The first is the improvement in adiabatic logic for low-power design. The other is the application of the inverters in 4-4 bit array multiplier.

The construction of the thesis is organized as following.

Chapter1 is the introduction which describes the developing of LSI, the emergence background of adiabatic logic which is suited to the Moore's law: the number of transistors in a dense integrated circuit doubles about every two years. As the number of transistors per unit area increases, the issue of energy consumption becomes more and more important. We briefly introduce the main power reduction methods from system level to device level. The motivation and organization of the thesis is followed.

Chapter 2 will describe the principle and classification of adiabatic logic. In this part, firstly, conventional CMOS inverter will be analyzed. And then, the adiabatic inverter comes. The difference of adiabatic inverter with CMOS inverter is that the conventional CMOS inverter uses the step voltage, while adiabatic inverter uses voltage power clock. The core principle of adiabatic logic is to return the electronic got from the power supply to it or release the energy stored in the node capacitance to the power supply by extending the process of electronics transform. As comparison, traditional CMOS inverter and the other adiabatic logic inverters will be analyzed in detail, i.e. CEPAL, 2N2N2P, ECRL and 2PASCL.

Chapter 3 contents the 2PC2AL inverter and proposed inverter. The 2PC2AL uses two-phase clocking split-level sinusoidal power supplies that minimize the voltage difference between the current-carrying electrodes, in other words, the energy consumption of the circuit can be suppressed. The simulation results show the correctness of lower energy loss. In the other hand, the circuit has a limitation of floating. Our research concentrates on eliminating on the phenomenon of floating adhering to the concept of low power consumption. Here we proposed one valid method to solve the floating: adding two switch transistors to prevent the voltage difference getting lower than the critical value. By choosing proper switch time, the floating can be resolved and the SPICE simulation result shows the low consumption characteristic of the proposed circuit compared to

CMOS inverter.

Chapter 4 explains the application of the proposed inverter. As basic component of digital circuit, we apply the inverter into NAND, full adder, half adder and 4-4 bit array multiplier. The simulation results show the correctness of logic function. To match the working clock, inverters are used in the input stage. By using 0.18μm CMOS technology, the multiplier made up of proposed inverter can realize the function correctly. The energy consumption of the static CMOS, 2PC2AL, proposed 2PC2AL, 2N2N2P and ECRL multipliers in one cycle are checked when the frequency ranges from 10 kHz to 100 MegHz. From the comparison we can see that the proposed multiplier has lower energy consumption compared to the CMOS multiplier.

Chapter 5 will draw the conclusion of the research. At the end of the thesis, prospective ideas of future works will be explored.