DOCTORAL DISSERTATION

Design and Implementation of Optoelectronic Receiver Analog Front-End in Low-Cost 0.18 μm CMOS Technology

March, 2020

Electronics and Information Systems Engineering Division
Graduate School of Engineering
Gifu University
Japan

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Design and Implementation of Optoelectronic Receiver Analog Front-End in Low-Cost 0.18 μm CMOS Technology

by

Xiangyu Chen

A Dissertation
Submitted in Partial Fulfillment of the Requirements
for the Degree of Doctor of Philosophy
in Engineering

Electronics and Information Systems Engineering Division
Graduate School of Engineering
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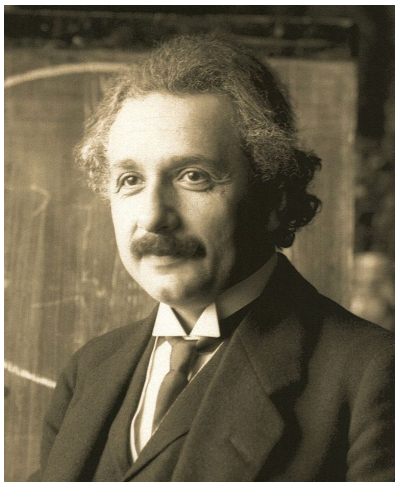
Japan

March, 2020

"Learn from yesterday,
live for today, hope for tomorrow.
The important thing is
not to stop questioning."



Albert Einstein (1879-1955)

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Abstract

With the continuous development of society and the continuous progress of science and technology, the exchange of information is increasing day by day, it is imperative to build a high-speed data transmission system. Optical fiber communication system has developed rapidly in response to this demand. It has been widely used for its advantages of high bandwidth and low attenuation. Optical receiver is of great importance in the entire optical system. In addition, front-end amplifier is the front part of optical receiver, which makes front-end amplifier an even more critical research topic.

In this thesis, a 15 Gb/s optical receiver trans-impedance amplifier (TIA) based on floating active inductor (FAI) for 10 G-PON deployments has been designed and implemented using a 0.18 μm CMOS process. The proposed TIA has a smaller area of 180 μm × 118 μm owing to floating active inductors based on gyrator-C structure and it is known from post-layout simulation results that it has power consumption of only 10.7 mW, transimpedance gain of 41 dBΩ and −3 dB frequency of 10 GHz with 0.15 pF total input capacitance. In order to achieve a complete optical communication analog front-end circuit, the author follow the the modified Cherry-Hooper differential amplifier as a post amplifier (PA) and a output buffer. The bandwidth of the proposed analog front-end circuit remains above 10 GHz.

Keywords: Optical receiver, Active inductor (AI), Transimpedance amplifier (TIA), Analog Front-End, Post amplifier (PA).

Declaration

The work in this thesis is based on research carried out at the Yasuhiro Takahashi Laboratory, Electronics and Information Systems Engineering Division, Graduate School of Engineering, Gifu University, Japan. No part of this thesis has been submitted elsewhere for any other degree or qualification and they are my own work unless referenced to the contrary in the text.

Acknowledgements

With the successful completion of the doctoral program, the student life of more than two decades will come to a successful conclusion. The five years of studying abroad in Japan, where I studied for a master's degree and a doctoral degree, have hone my patience and made me more hardworking. I would like to express my gratitude for all the help and support that I have received.

First and foremost, I would like to offer my special thanks to my parents, Degui Chen and Ping Zhao, who supported me to study in Gifu University, and have always encouraged and believed in me. Their unconditional love supported me in completing this great project.

There is a famous saying in China called "Even if someone is your teacher for only a day, you should regard him like your father for the rest of your life". This dissertation could not have been completed without the patient and intensive supervision, valuable technical opinion and deeply discussion of Associate Prof. Dr. Yasuhiro Takahashi, my supervisor. Therefore, I would like to take this opportunity to show my greatest appreciation to Dr. Yasuhiro Takahashi. I would also like to thank Associate Prof. Dr. Toshikazu Sekine, the supervisor of my master's degree program, who patiently taught me how to research when I first arrived in Japan.

I thank all the members of Takahashi laboratory in Gifu University for the daily discussion on this work.

I would also like to acknowledge the financial support by the China Scholarship Council (CSC) through the award of a Ph.D. scholarship (No. 201808050092) to Xiangyu Chen, which is under the State Scholarship Fund. It was CSC's financial support that allowed me to focus on my research without any thoughts.

I acknowledge that this work was supported by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Cadence Corporation and Synopsys, Inc. The VLSI chip in this study has been fabricated in the chip fabrication program of VDEC, the University of Tokyo in collaboration with Rohm Corporation and Toppan Printing Corporation.

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Chapter 1

Introduction

1.1 Research Significance and Background of the Subject

Human beings have entered the internet era for nearly 30 years. The internet technology based on computer technology and communication technology has been developing rapidly. Today, this trend has not slowed down, but changed its development form, because the world is changing from the internet age to the intelligent age. More and more parts of people's work and life are being assisted by intelligent devices. The artificial intelligence industry represented by big data, Internet of things, cloud computing, intelligent brain, intelligent mobile terminals, wearable devices and intelligent home is rapidly rising [1–7]. In terms of software or hardware, one of the important factors that determine the performance of intelligent products is the speed of information transmission and processing. As shown in Fig. 1.1, overall IP traffic is expected to grow to 396 EB per month by 2022, which is over three times the 2017 rate, lead by the increased use of IoT device traffic, video, and sheer number of new users coming onboard, a compound annual growth rate (CAGR) of 26 percent [8].

A slew of applications from smart meters, video, healthcare monitoring, smart car communications, and more will continue to contribute to a significant growth in traffic. Therefore, the development of communication technology still has an important impact on the technological development process of the intelligent age. According to Cisco, the internet giant, since 1984, over 4.7 ZB of IP traffic have flowed across networks, but that's just a hint of what's coming. By 2022, more IP traffic will cross global networks than in all prior "internet years" combined up to the end of 2016. In other words, more traffic will be created in 2022 than in the first

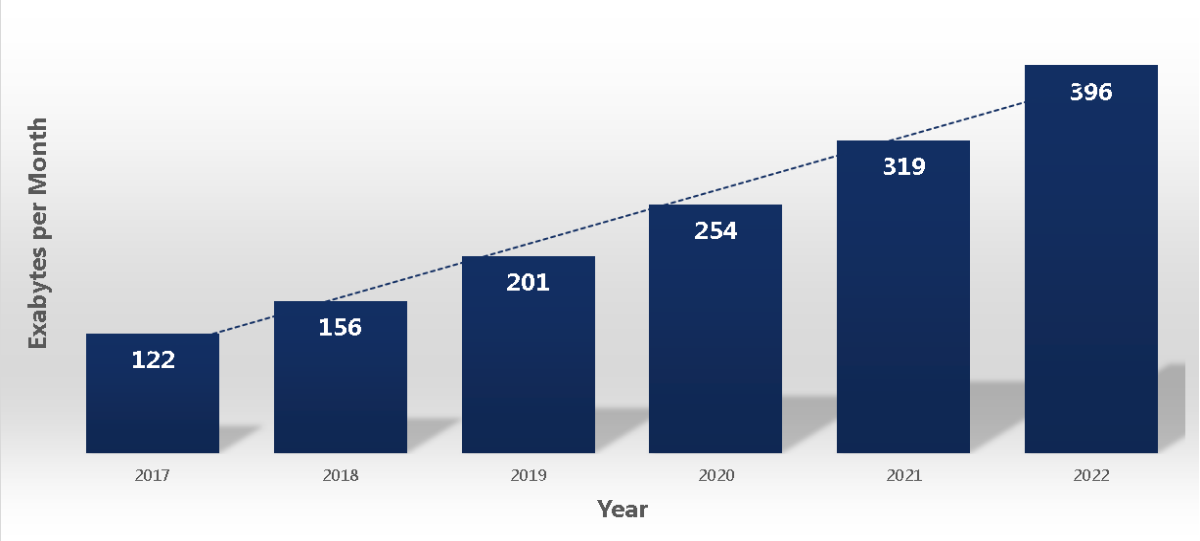


Figure 1.1: Forecast of monthly IP traffic by 2022 [8].

32 years since the internet started [8].

In the development of communication network technology, the short-distance communication network technology which is mainly connected by electric interconnection has played an important role. With the continuous increase of information traffic in modern communication networks, the data rate between nodes in the system is gradually approaching the physical limit of general links such as copper wires. Therefore, it is urgent to find a transmission medium with higher communication speed and capacity. Optical fiber communication is an advanced communication mode that relies on optical fiber as transmission medium and optical wave as carrier. In essence, light waves are electromagnetic waves of very high frequency. Therefore, optical fiber communication with a large capacity of light wave as the carrier is ten thousand times more than other means of ommunication at present. It can be inferred that the development of optical fiber communication is the inevitable trend of the communication industry. Compared with microwave and cable communication, optical fiber communication shows many advantages, such as lower transmission loss, longer relay distance, wide transmission band and great communication capacity. Fiber optical communication with quartz as the raw material, save copper (aluminum), lead and other raw materials. In addition, optical fiber communication has strong confidentiality, corrosion resistance and radiation resistance; hence it is often used in special environment. Therefore, research on optical communication system is the direction of our efforts [9–28].

The optical link system urgently needs the optical receiver front end with high

sensitivity, wide dynamic range and reasonable bandwidth to detect the tiny photocurrent generated by the photodiode and convert it into large voltage for further signal processing. However, in the commercial phase, low power consumption and more portable should also be considered [29, 30]. The proliferation of internet access and data communication has driven the required system bandwidth to increase rapidly, and thus 50 Gb/s levels optical transport systems with SiGe, GaAs, and InP technologies have recently been paid a great deal of attention. However, optical receivers with lower power consumption and smaller size at the data rate of 10-20 Gb/s are still of interest for the commercial 10 G-PON/10 G-EPON deployments increasing. Figure 1.2 shows the actual application position of our target 10 G-PON in the entire commercial optical communication network. Furthermore, compared to expensive process technologies such as SiGe, GaAs, etc., low-cost and highly integrated CMOS technology is still the focus of commercial passive optical network [31, 32].

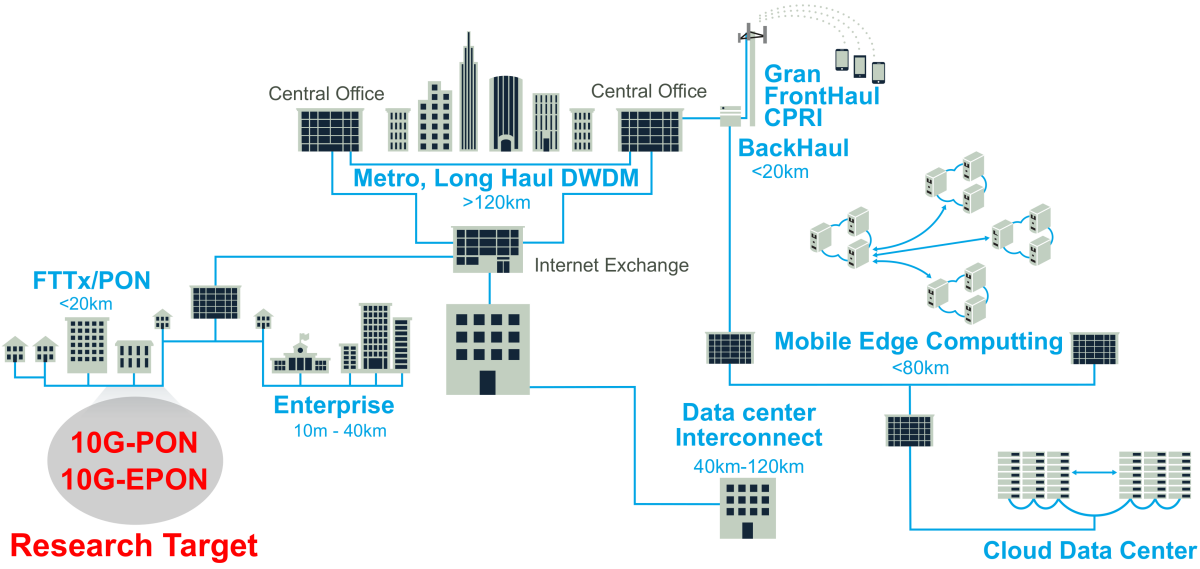


Figure 1.2: Application position of our target 10 G-PON and the commercial optical communication network.

1.2 Generic Optical Cmmunication Building Blocks

The goal of an optical communication system is to carry large volumes of data across a long distance. For example, the telephone traffic in Europe is connected to that in the United States through a fiber system installed across the Atlantic Ocean.

Depicted in Fig. 1.3, a generic optical communication system consists of three components: (1) an optical transmitter, which converts the electrical data to optical form; (2) a fiber, which carries the light produced by the laser; and (3) an optical receiver, which senses the light at the end of the fiber and converts it to an electrical signal.

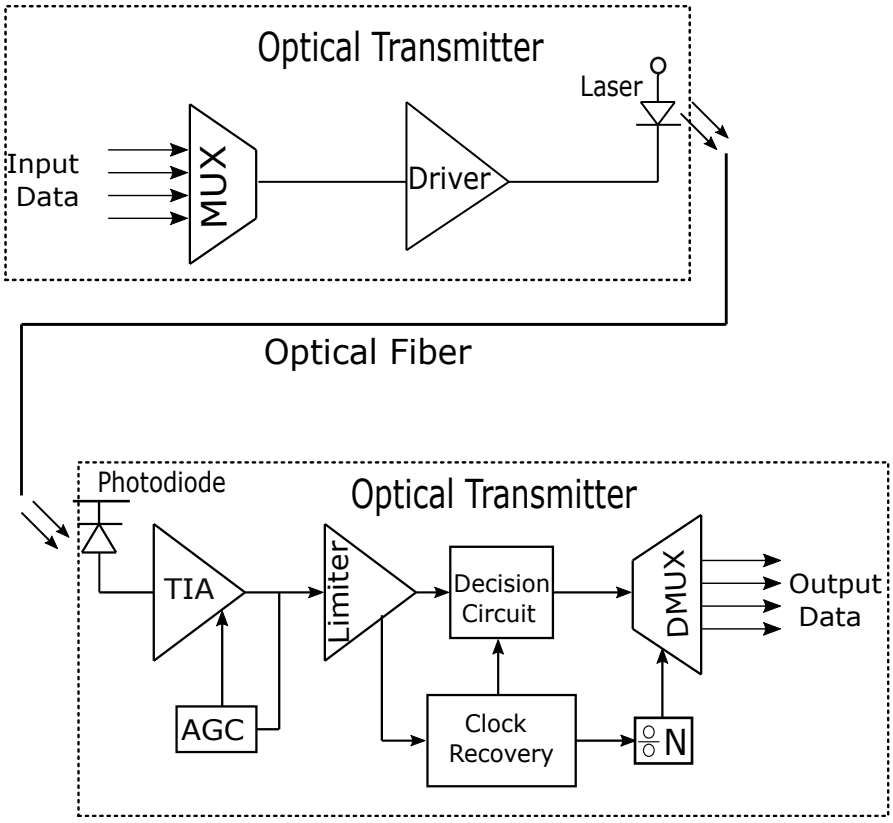


Figure 1.3: Block diagram for an optical communication system.

On the transmitter side a time-division multiplexer (MUX) combines N parallel low data rate streams into a fast serial data stream with N times higher bit rate. A laser driver drives the laser diode or a modulator driver drives a modulator. The laser driver modulate the current of a laser diode. The modulator driver modulates the voltage across a modulator, which in turn modulates the light intensity from a continuous wave laser. Laser diodes convert electronic signals into optical ones. The optical signal emitted from the laser is coupled to the optical fiber and propagates over the optical fiber to the optical receiver.

On the receiver side, the photodiode receives the optical signal coupled from the optical fiber and converts it to an electrical current signal. The current signal generated by the photodiode is usually small due to the fiber attenuation after

long distance and the low responsivity for the photodiode in nanometer CMOS technology. The photodiode is connected to a transimpedance amplifier (TIA) to convert and amplify the photocurrent into a voltage signal. The TIA should give high gain, wide bandwidth and low noise. Automatic gain control (AGC) can be used to make TIA work at high input photocurrents; increasing the dynamic range. The output voltage swing of the limiting amplifier (LA) is kept constant independent of the input signal level which is working with binary data formats. The clock recovery circuit retrieves the clock from data which is needed for the decision circuit and DMUX. The decision circuit regenerates the high quality data to reduce the effects of limited bandwitdh and timing jitter produced by the cascaded amplifiers. The DMUX splits the serial high data rate stream back into the original N parallel low bit rate streams [33–35].

1.3 Motivation of this Research

This work analyzes and summarizes the conventional transimpedance amplifier (TIA) and post amplifier (PA) which is operated as limiting amplifier (LA) bandwidth expansion technologies, such as matching LC network, regulated cascode (RGC) input stage, and a capacitive degeneration stage. It is well known that, there are several works that have been reported to improve the bandwidth of TIA. Inductive peaking has been extensively used to improve the bandwidth and decrease parasitic capacitance effects. Inductor is one of the most important TIA elements for high frequency application and RF systems. However, an extreme size of the inductor makes the chip large and costly. As a result, decreasing the area of required inductors for TIA design is very important. An floating active inductor (FAI) is constructed using a small number of transistors for the gyrator realization. The transistor based FAI is developed using two differential transconductors connected back to back in a negative feedback configuration.

This thesis describes the results of design and implementation of an analog front-end TIA for optical communications with low power consumption characteristics and small area. The demand for large-capacity communication on the internet is still very high, and there is a demand for higher performance and lower power consumption of such a large-capacity optical communication system integrated circuit. This design is mainly used for the commercial 10G-PON/10G-EPON that pursue miniaturization and low energy consumption. The proposed TIA with a floating active inductor not only has the advantages of large bandwidth of 10 GHz and tran-

simpedance gain of 41 dBΩ, but also has the advantages of smaller chip area and lower power dissipation compared with conventional TIAs using a spiral inductor. In order to make the gain more desirable, the TIA must followed by additional amplifying stages that boost the signal swing to logical levels. In our proposed front-end circuit, a modified Cherry-Hooper amplifier with resistive loads is used, which cascades an output buffer. Since Cherry-Hooper amplifier is a differential structure, we used an unbalanced pseudo-differential TIA with one photodector for matching. This unbalanced pseudo-differential TIA consists of a single-ended main TIA and a matched replica TIA (a.k.a. dummy TIA). The replica TIA simply produces a DC voltage that tracks the dark level of the signal voltage over process, voltage, and temperature. The proposed analog front end circuit achieves a gain of 70 dBΩ and maintains a bandwidth above 10 GHz.

1.4 Organization of the Dissertation

This thesis consists of the following five chapters:

Chapter 1 (this chapter) is the introduction which describes the background, generic optical communication system, motivation of this research and organization of the dissertation.

In Chapter 2, the author discusses the basics of an analog front-end circuit for an optical receiver including TIA and LA. In addition, the TIA can be categorized into two main topologies: the open loop TIAs and the shunt-shunt feedback TIAs.

Chapter 3 describes the the basic theory of floating active inductor (FAI) and discusses Mahmoudi and Salama floating active inductor in detail.

Chapter 4 introduces in detail the design process and topology of the proposed TIA, including the choice of broadband enhancement technology, the simulation analysis of the selected floating active inductor, and the noise analysis of the proposed TIA. Finally, the post-layout simulation results are shown and compared with other TIAs. The author also presents a proposed optical receiver analog front-end circuit composed of the proposed TIA with CMOS floating active inductor, a modified Cherry-Hooper amplifier and an output buffer.

Finally, the conclusions and future works are drawn in Chapter 5.

Chapter 2
Basic Fundamentals of Optical Communication Receiver

2.1 General Architecture of Optical Communication Receiver

The basic structure of the general optical communication receiver is shown in Fig 2.1, which mainly includes three parts: (1) photodiode; (2) analog front-end circuits, including TIA, PA and output buffer; (3) clock recovery, decision circuit and DMUX.

Photodiode is very important to the performance of the optical receiver, it directly affects the noise, speed and sensitivity of the whole receiver. Generally speaking, the photodiode will introduce a relatively large capacitance at the input of the TIA. This capacitance will directly affect the speed of the receiver; hence the research of low parasitic capacitance photodiode is very important for high-speed optical communication receivers.

The main function of the analog front-end circuit is to convert the photo-current into a voltage and amplify it to a certain swing, so that the CDR can correctly recover the clock and data, and subsequent digital processing circuits can process it. The current signal generated by the photodetector is usually small due to the fiber attenuation after long distance and the low responsivity for the photodetector in nanometer CMOS technology. The photodetector is connected to a TIA to convert and amplifiey the photo-current into a voltage signal. The TIA should give high gain, wide bandwidth and low-noise. Since the TIA output swing may not be large enough to provide logical levels, a high-gain amplifier (called a "limiting amplifier (LA)") must follow the TIA. LA is responsible for further amplifying the signal,

and transforming the low-swing irregular waveform of the TIA output into a square wave with a high swing rule. Since the input impedance of the test equipment is 50 Ω, the buffer stage provides 50 Ω impedance matching while providing sufficient drive capability.

Moreover, since the received data may exhibit subtantial noise, a clean-up flipflop (called a "decision circuit") is interposed between the LA and the DMUX. The clock must bear a well-defined phase relationship with respect to the received data so that the flipflop samples the high and low levels optimally, i.e., at the midpoint of each bit. The task of generating such a clock from the incoming data is called "clock recovery". The overall operation of clock recovery and data cleanup is called "clock and data recovery" (CDR) [34].

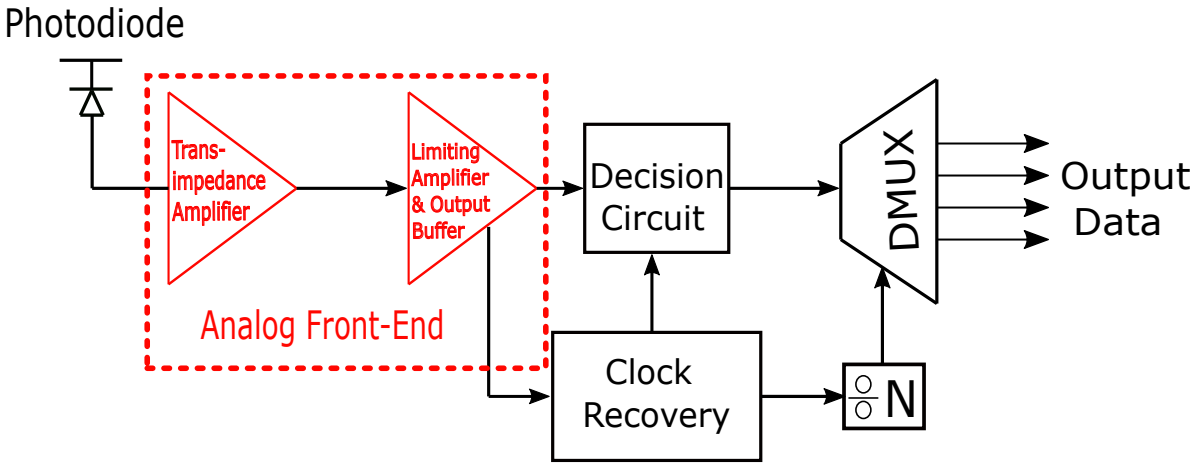


Figure 2.1: General architecture of optical communication receiver.

2.2 Optical Receiver Characteristic Parameters

- **Binary Data Formats:** The non-return-to-zero (NRZ) and return-to-zero (RZ) formats are the most commonly used modulation formats in optical communication systems, see the example shown in Fig 2.2. For NRZ the signal is high transmit ONE bit and is low to transmit a ZERO bit. When the signal is high, it stays high for the entire bit period T. The inverse of the bit period is the data rate. The transmitted data is random in nature and the ONE and the ZERO occur typically with an equal probability. For RZ format, the bits ONE, occupy only half of the bit period. The RZ format requires less signal to noise ratio compared with the NRZ. Due to the narrower pulse width of

RZ, the effect of pulse spreading on adjacent bits is negligible. On the other hand, RZ has wider bandwidth due to shorter pulses, therefore RZ requires wider bandwidth circuits [34, 35].

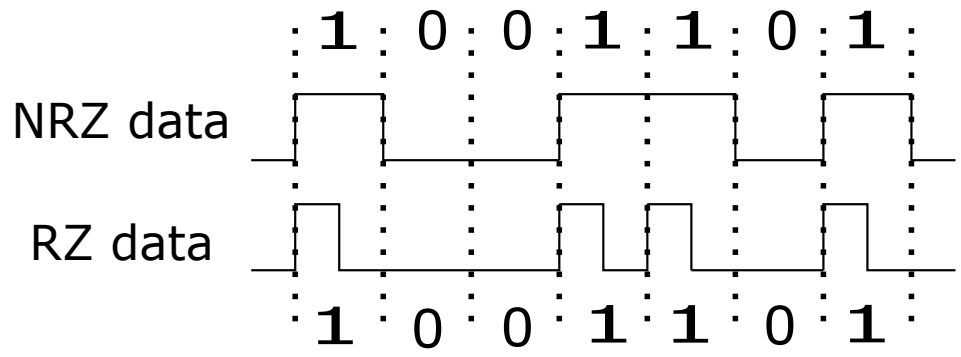


Figure 2.2: NRZ and RZ data fomats.

- **Transimpedance Gain (for TIA):** The input end of TIA is the current signal and the output end is the voltage signal. That is, the gain of a circuit is the ratio of its output voltage to its input photo-current current. It is expressed by:

$$G_{\mathrm{TIA}} = \frac{V_{out}}{I_{ph}} \quad (\Omega), \tag{2.1}$$

where I_{ph} is a current of photodiode. The transimpedance gain of TIAs must be large enough to overcome the noise of the subsequent stage.

- **Gain (for LA):** Since the output signal of the TIA is inadequate for the CDR circuits, an LA is supposed to be interposed between the TIA and the CDR circuits. In order to boost the signal swing produced by the TIA to a required level and to minimize the noise contributed by the following stages, the LA must provide enough gain.

- **Input-Referred Noise Current:** The input-referred noise current is one of the most important parameters of TIA. The noise of TIA is generally more significant than other noise sources such as photodiodes and limiting amplifiers, so that it usually determines the sensitivity of the optical receiver, that is, the lower limit of the input dynamic range of the optical receiver. Figure 2.3 shows a noiseless transimpedance amplifier with an equivalent noise

current source $I_{n,TIA}$ at the input end. The noise current source and the ideal noiseless transimpedance amplifier constitute a practical transimpedance amplifier model. The equivalent noise current source $I_{n,TIA}$ is also referred to as the input reference noise current. The power spectral density $I^2_{in,TIA}(f)$, also known as the input-referred noise current spectral density, is shown in Fig 2.4.

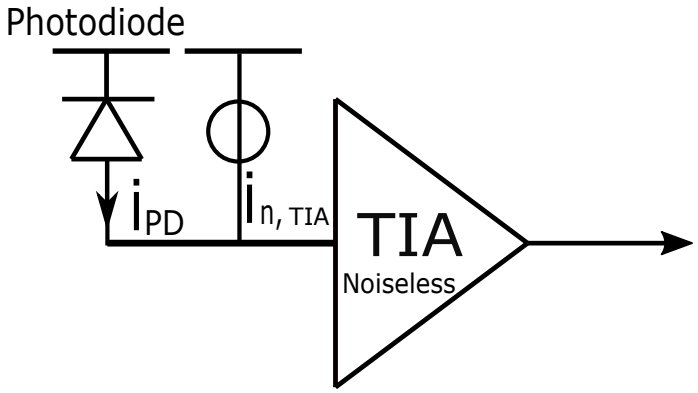


Figure 2.3: Model of Input Referred Noise Current.

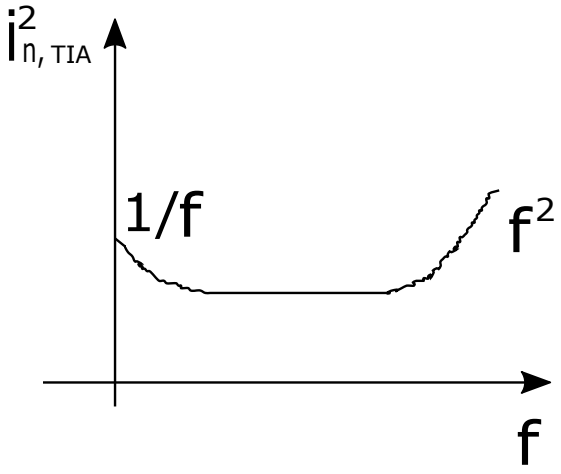


Figure 2.4: Typical Power Spectrum.

The power spectral density is expressed as $\mathrm{pA}^2/\mathrm{Hz}$. In more cases, take the square root of it $I_{in,TIA}(f)$, and use $\mathrm{pA}/\sqrt{\mathrm{Hz}}$ as its quantized unit.

- **Sensitivity:** Sensitivity is one of the most important performance indicators of optical receiver. It is defined as the minimum average optical power (P_{min}) that an optical receiver can receive while ensuring a certain bit error rate (BER). It is usual to calculate the sensitivity in dBm, the equation for

calculating sensitivity for a certain BER is as follows:

$$Sensitivity = 10log\frac{P_{min}}{1mW}dBm, \tag{2.2}$$

The unit of P_{min} is W, which can be defined as:

$$P_{min} = \frac{QI_{in,noise}}{R}, \tag{2.3}$$

where Q is the signal-to-noise ratio, and R is the responsivity of the photodiode. It can be known from Equations (2.2) and (2.3) that when the signal-to-noise ratio is determined, the responsivity of the photodetector and the Input-Referred Noise Current $I_{in,noise}$ become the main factors affecting the sensitivity.

- **Intersymbol Interference (ISI) and Bandwidth (BW):** Bandwidth (BW) is defined as the upper frequency where the gain drops -3 dB below its mid-band value. In general, BW is limited by the total capacitance contributed by the photodiode and other parasitic elements existing at the optical front-end. If the circuit bandwidth is lower than the bandwidth of the input signal, then the output signal rise/fall time and the amplitude will be affected. the rise/fall time will increase and the fast bits will have a tail that will affect amplitude of the adjacent bits. The influence of adjacent bits on the amplitude of the output signal is called intersymbol interference (ISI). Alternatively, if the receiver bandwidth is wide enough such that the signal waveform remains undistorted, the signal picks up a lot of noise, which translates into a low receiver sensitivity. As a rule of thumb, the optimum -3 dB BW for non-return-to-zero (NRZ) receivers is about 60 to 70 % of the bit rate (BR),

$$BW \approx 0.6BR...0.7BR, \tag{2.4}$$

or $BW \approx \frac{2}{3}BR$ to pick a specific number in this range [36].

- **Jitter:** The decision threshold voltage slices the eye diagram horizontally. Jitter is the deviations of the threshold voltage crossings from their ideal position in time. Jitter is important when dealing with systems operating at high data rates or systems requiring precise clocks. The jitter in the time domain is

called phase noise in the frequency domain. As jitter increases the horizontal eye opening is decreasing and a bit error can occur. In the following section, the author will show how to see the jitter in the eye diagram.

- **Eye Diagram:** Eye diagrams provide an intuitive graphical representation of electrical or optical digital communication signals. the quality of the signal, that is, the rise/fall times, the amount of ISI, noise, and jitter, can be judged from the appearance of the eye [36]. Figure 2.5 shows a typical eye diagram, which includes the jitter, horizontal eye opening, decision threshold voltage and smpling instant.

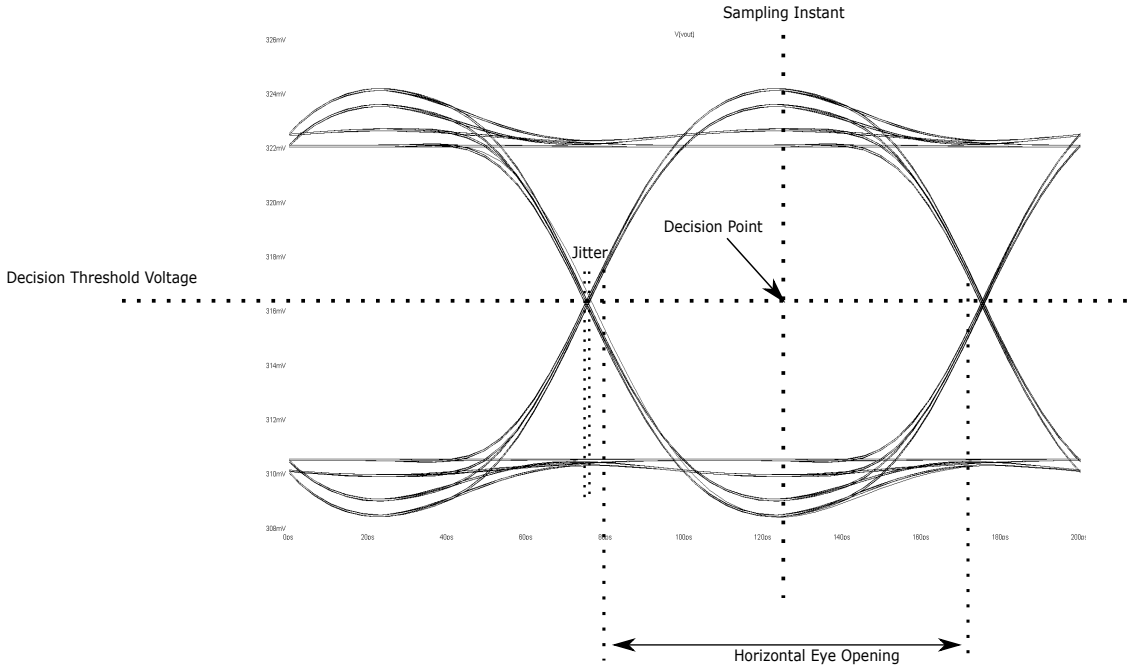


Figure 2.5: Typical eye diagram.

2.3 Topologies of Trans-impedance Amplifier (TIA)

Current-to-voltage converters are necessary in optical receivers in order to convert and amplify the weak photo-current delivered by the photodiode into a strong output voltage signal which is proportional to the input current. The trans-impedance amplifier (TIA) is the most suitable preamplifier structure for optical receivers. An optical communication system like Ethernet Passive Optical Network (10G-EPON) needs a broadband TIA with a high sensitivity. The preamplifier is considered to be the most important component of the optical receiver because its performance

is largely determined by the performance of the entire optical receiving system. Generally, there are two types of TIA topologies, such as open loop and feedback TIAs [35].

2.3.1 Open Loop TIAs

The open loop TIAs like common-gate (CG), regulated cascode (RGC), and inverter common drain feedback (ICDF) TIAs will be introduced in this section. The common-gate configuration relaxes the effect of large input parasitic capacitance on the bandwidth. However, the poor device characteristics of nanometer MOSFET cannot totally isolate the parasitic capacitance. The CG-TIA's noise performance is worse than for the common-source (CS) TIA with shunt feedback. The CG-TIA's noise performance cannot be optimized without scarfing the power dissipation. The regulated cascode (RGC) TIA has a very low input impedance which can support a wide bandwidth at low power dissipation but the noise performance is still worse than that of the CS-TIA with shunt feedback. The ICDF-TIA shows a higher performance compared to the RGC-TIA.

1. **Common Gate Input Stage:** Open-loop TIAs often use a common gate or common base topology, mainly because of its low input impedance. Figure 2.6 shows the typical common gate TIA. The transistor M_1 in common gate operations with a resistive load R_D. Since all of the photodiode currents

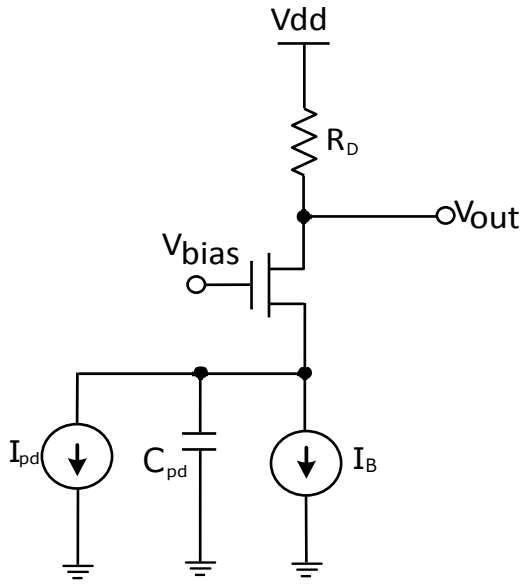


Figure 2.6: Common Gate TIA circuitry.

pass through the load resistance R_D, The low frequency transimpedance gain of CG-TIA is expressed by:

$$Z_{\mathrm{T}}(\mathrm{CG})(0) \approx \mathrm{R_D}. \tag{2.5}$$

The input resistance of this amplifier is given by:

$$Z_{\mathrm{in}}(\mathrm{CG}) \approx \frac{r_{ds1} + R_D}{1 + (g_{m1} + g_{mb1})r_{ds1}}, \tag{2.6}$$

where r_{ds1} is the drain to source resistance, g_{m1} is the device transconductance, and g_{mb1} is the back-gate transconductance due to the body effect. For long channel devices operating in the saturation region, the value of r_{ds} is large and this equation reduces to the following relationship, where the input resistance is only dependent on the properties of the device and is independent of the load resistance R_D as follows:

$$Z_{\mathrm{in}}(\mathrm{CG}) \approx \frac{1}{g_{m1}}. \tag{2.7}$$

The bandwidth of the CG-TIA can be determined by:

$$BW(\mathrm{CG}) = \frac{\mathrm{g_{m1}}}{2\pi \mathrm{C_{pd}}}. \tag{2.8}$$

2. **Regulated-Cascode (RGC) TIA:** Figure 2.7 shows the circuitry of a RGC TIA. The photo-current is converted to a voltage at the drain of M_1. The stage consisting of M_2 and R_2 operates as a local feedback and thus reduces the input impedance by the amount of its own voltage gain. It can be seen that the RGC-TIA has a very low input impedance and can support wide bandwidth at low power disspation. The capacitive effects can be isolated using RGC configuration. Figure 2.8 shows the small-signal equivalent circuit of the RGC-TIA taking into consideration the effect of channel length modulation.

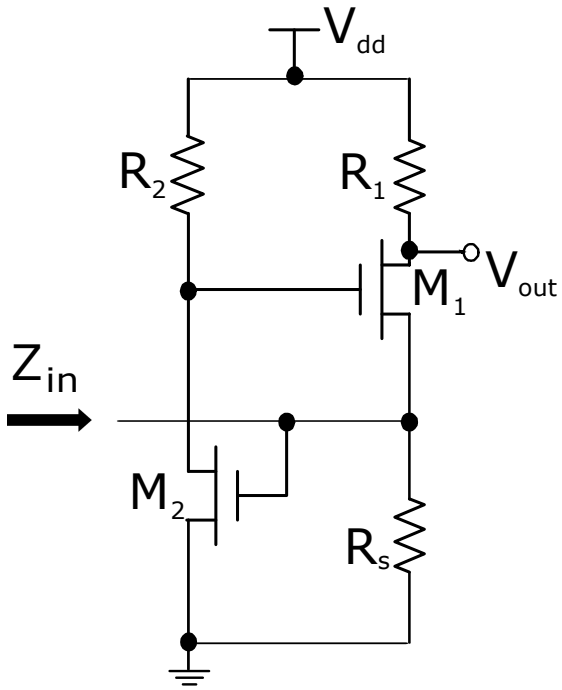


Figure 2.7: RGC TIA circuitry.

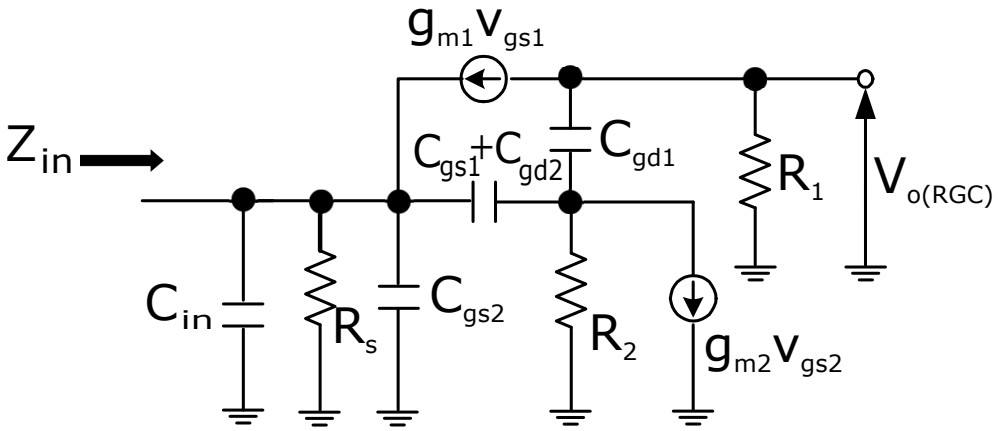


Figure 2.8: RGC TIA small-signal equivalent circuit.

The low frequency transimpedance gain of RGC-TIA is given by:

$$Z_{\mathrm{T}}(\mathrm{RGC})(0) \approx \mathrm{R}_1, \tag{2.9}$$

We can see from the two expressions of Equations (2.5) and (2.9) that the gains at low frequency of the two TIAs are almost the same. The RGC bandwidth determined by the dominant pole is

$$BW(\mathrm{RGC}) = \frac{\mathrm{g_{m1}(g_{m2}R_2 + 1)}}{2\pi \mathrm{C_{in}}}. \tag{2.10}$$

Compared with the CG-TIA's bandwidth of Equation (2.8), the RGC bandwidth is increased by the factor $(g_{m2}R_2 + 1)$ for the same g_{m1}. According to the small-signal analysis, the input resistance of the RGC circuit is given by:

$$Z_{\mathrm{in}}(\mathrm{RGC}) \approx \frac{1}{g_{m1}(g_{m2}R_2 + 1)}. \tag{2.11}$$

It is clearly seen that the input impedance of RGC is $(g_{m2}R_2+1)$ times smaller than that of a CG input TIA. In other words, RGC input stage can be essentially equivalent to a CG TIA with a large transconductance of $g_{m1}(1+g_{m2}R_2)$. The main advantage of the RGC input stage is that the input impedance is low and the effect of the larger photodiode capacitance can be isolated. Compared to the bandwidth of the common gate stages, the RGC bandwidth can be increased for the same transconductance of M_1. For the same bandwidth a CG stage needs a higher g_{m1} than the RGC stage which means a larger current is needed through M_1. The power disspation of the RGC stage is lower than that of the CG stage. The RGC transimpedance gain is limited by R_1 which cannot be increased due to limited low supply voltage.

2.3.2 Shunt-shunt Feedback TIA

Shunt-shunt feedback TIA is basically a current-voltage converter with negative resistance feedback, which is a very common circuit topology in optical fiber applications. This parallel feedback configuration provides wide bandwidth by reducing the input impedance while maintaining large resistance values in the feedback loop to enhance noise performance.

Figure 2.9 shows a schematic of a shunt-shunt feedback TIA. The trans-impedance

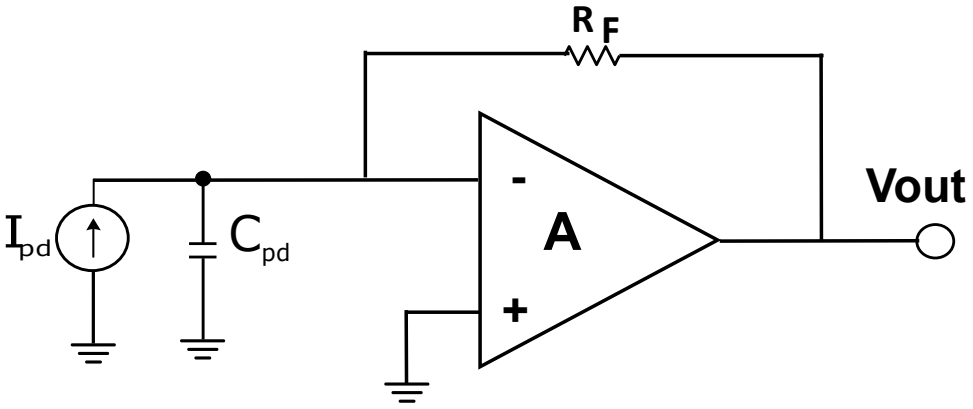


Figure 2.9: Basic circuit of shunt-shunt feedback TIA.

of the shunt-shunt feedback TIA can be approximated as:

$$Z_{\text{TIA}} = \frac{R_F}{1 + j2\pi f(R_F C_{pd} A)(1 + j2\pi R_{out})}. \tag{2.12}$$

If we assume that the dominant pole is placed at the input, the bandwidth can be expressed as:

$$BW_{\text{TIA}} = \frac{A}{2\pi C_{pd} R_F}. \tag{2.13}$$

2.4 Basic of Post Amplifiers (PA)

The output signal from the TIA is in the range of a few millivolts and more gain is needed to reach at least an amplitude of 200 mV required by the decision circuit. The additional gain will be introduced by the PA following the TIA. As stated in section 4.1, the TIA specifications determine the performance of the optical receiver. The PA specifications have less impact, but insufficient PA bandwidth, gain, and sensitivity can degrade the optical receiver's overall performance. There are two main types of post amplifier (PA), the limiting amplifier (LA) and the automatic gain control (AGC) amplifier. The selection of LA or AGC amplifier depends on the required system performance, like linearity, gain and sensitivity.

The LA is easier to design than an AGC amplifier as it does not have an AGC. The LA has a fixed gain which can be considered as the maximum gain value of

the AGC amplifier, so the LA performance (like sensitivity, bandwidth and power disspation) will be better than the AGC amplifier's performance.

Chapter 3
Principle of CMOS Floating Active Inductors

3.1 CMOS Active Inductors

Inductors are one of the most important circuit components in high-frequency applications and RF systems. However, although the traditional spiral inductor has a good quality factor, it is often criticized because of its huge volume, which increases the use cost. Recently, CMOS inductors and transformers have found a broad range of applications in high-speed analog signal processing including impedance matching and gain-boosting in wireless transceivers, bandwidth inprovement in broadband data communications over wire and optical channels, oscillators and modulators, RF bandpass filters, RF phase shifters, RF power dividers, and coupling of high-frequency signals, etc. Inductors and transformers synthesized using active devices, known as active inductors and transformers, offer a number of unique advantages over their spiral counterparts including virtually no chip area requirement, large and tunable inductances with large tuning ranges, large and tunable quality factors, high self-resonant frequencies, and full compatibility with digital oriented CMOS technology [37].

An active inductor is constructed using small number of transistors for the gyrator realization. The transistor based active inductor is developed using two differential transconductors connected back to back in a negative feedback configuration. The parasitic capacitance of the basis transistors is used as the load capacitance to realize a Gyrator-C topology. The gyrator-C active inductors are mainly divided into two categories according to the topology, namely single-ended gyrator-C active inductors and floating gyrator-C active inductors.

3.1.1 Lossless Single-Ended Gyrator-C Active Inductors

The gyrator consists of two transconductors connected back to back. When one port of the gyrator is connected to a capacitor, as shown in Fig. 3.1, the network is called the gyrator-C network. G_{m1} and G_{m2} are refer to the output current of transconductors 1 and 2, respectively, and C is the load capacitance at node 1. The gyrator-C network is considered lossless when the input and output impedances of the transconductors of the network are infinite and the transconductances of the transconductors are constant. Considering the lossless gyrator-C network shown in Fig. 3.1, Equation (3.1) gives the admittance of port 2 of the gyrator-C network as:

$$Y = \frac{I_{in}}{V_2} = \frac{1}{s(\frac{C}{G_{m1}G_{m2}})}. \tag{3.1}$$

Equation (3.1) indicates that port 2 of the gyrator-C network behaves as a single-ended lossless inductor with its inductance given by Equation (3.2).

$$L = \frac{C}{G_{m1}G_{m2}}. \tag{3.2}$$

Therefore, Gyrator-C networks can be used to synthesize inductors.

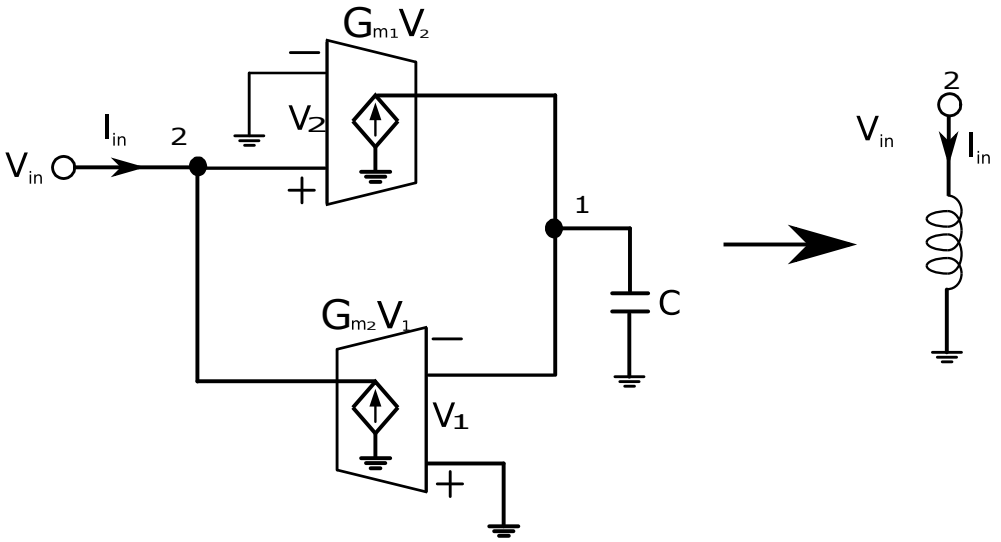


Figure 3.1: Lossless single-ended gyrator-C active inductors.

3.1.2 Lossless Floating Gyrator-C Active Inductors

An inductor is said to be floating if both the terminals of the inductor are not connected to either the ground or power supply of the circuits containing the active inductor. Floating gyrator-C active inductors can be constructed in a similar way as single-ended gyrator-C active inductors by replacing single-ended transconductors with differentially-configured transconductors.

An active inductor is constructed with a small number of transistors for the implementation of the the gyrator. The gyrator consists of two back-to-back connected transconductors [37]. When the port of gyrator is connected to a capacitor, as shown in Fig. 3.2, the network is called the gyrator-C network. A gyrator-C network is said to be lossless when both the input and output impedances of the transconductor of the system are infinite, and the transconductances of the transconductors are constant. For node A and node B, we have:

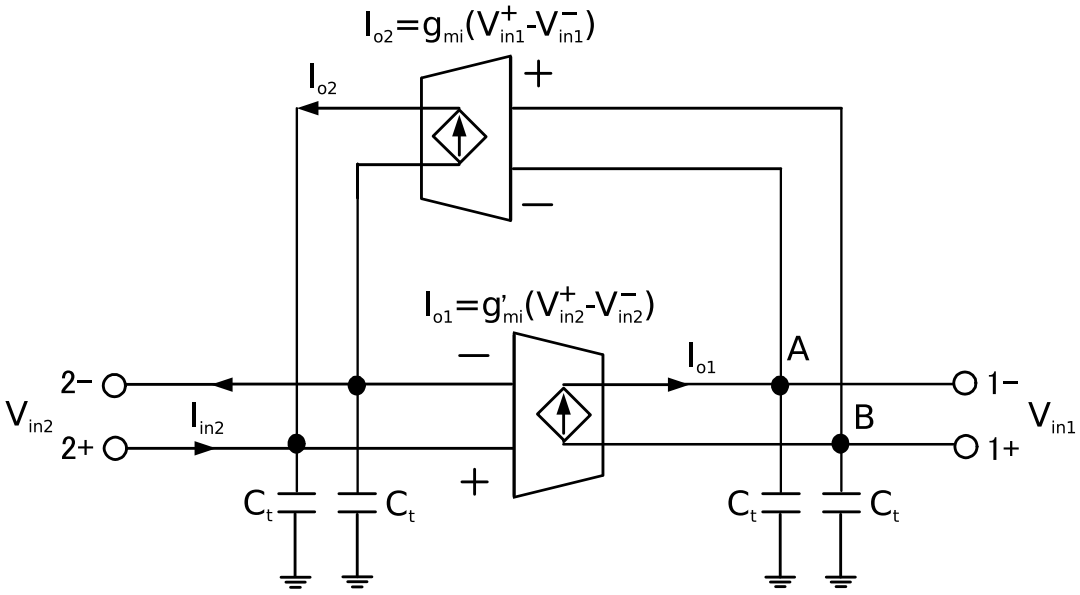


Figure 3.2: Lossless floating gyrator-C active inductors.

$$V_A = V_{in1}^- = -\frac{g'_{mi}}{sC_t}\left(V_{in2}^+ - V_{in2}^-\right), \tag{3.3}$$

$$V_B = V_{in1}^+ = \frac{g'_{mi}}{sC_t}\left(V_{in2}^+ - V_{in2}^-\right), \tag{3.4}$$

$$I_{o2} = g_{mi}\left(V_{in1}^+ - V_{in1}^-\right). \tag{3.5}$$

Here, we substitute Equations (3.3) and (3.4) into Eq. (3.5), we have

$$I_{o2} = \frac{2g_{mi}g'_{mi}}{sC_t}\left(V^+_{in2} - V^-_{in2}\right). \tag{3.6}$$

In this network, we can write

$$I_{in2} = -I_{o2}. \tag{3.7}$$

The admittance looking into port 2 of the gyrator-C network is given by

$$\begin{aligned} Y &= \frac{\frac{2g_{mi}g'_{mi}}{sC_t}\left(V^+_{in2} - V^-_{in2}\right)}{V^+_{in2} - V^-_{in2}} \\ &= \frac{2g_{mi}g'_{mi}}{sC_t} \\ &= \frac{1}{s\left(\frac{\frac{C_t}{2}}{2g_{mi}g'_{mi}}\right)}. \end{aligned} \tag{3.8}$$

Equation (3.8) reveals port 2 of the gyrator-C network behaves as a floating inductor with its inductance given by

$$L = \frac{\frac{C_t}{2}}{g_{mi}g'_{mi}}. \tag{3.9}$$

3.2 Mahmoudi and Salama Active Inductor

The floating active inductor proposed by Mahmoudi and Salama is used in the design of quadrature down converters for wireless applications [38, 39]. The schematic of the the floating active inductor is shown in Fig. 3.3. It mainly consisted of a pair of differential transconductors and a pair of negative resistors at the output of the transconductors. M_8 and M_{16} are biased in the triode and behaved as voltage controlled resistors. They are added to the conventional cross-coupled configuration of negative resistors to provide resistance tunability for the negative resistors, without using a tail current source. The common-mode stabilizer consists of a cross-coupled differential pair M_6, M_7 (M_{14}, M_{15}) and transistor M_8 (M_{16}), which is designed to operate in triode mode. The stabilizer is added to the design to stabilize the common-mode behavior of the differential active inductor by moving the common-mode right half-plane pole of the inductor, which may cause instabil-

ity, to the left-half-plane. In the differential mode of operation, the common-mode stabilizer appears as an impedance Z_o with a real part given by [40]:

$$\mathrm{Re}\{\mathrm{Z_o}\} = -\frac{1}{\mathrm{g_{ms}}}||\mathrm{r_{os}}, \tag{3.10}$$

where g_{ms} is the transconductance of M_6 or M_7 and r_{os} is the output resistance of M_8 in the triode region, which can be controlled by the voltage V_{b3}. Hence, the stability of the active inductor is improved.

Figure 3.4 shows clearly that the Mahmoudi–Salama FAI is based on the gyrator-C structure. According to the inductance relationship of Equation (3.9), when the gyrator-C network appeared as a FAI described in Subsection 3.1.2, we could obtain:

$$L = \frac{C}{g_{mi}g'_{mi}}, \tag{3.11}$$

where g_{mi} and g'_{mi} are the transconductances of M_{10} (M_{11}) and M_2 (M_3), respectively.

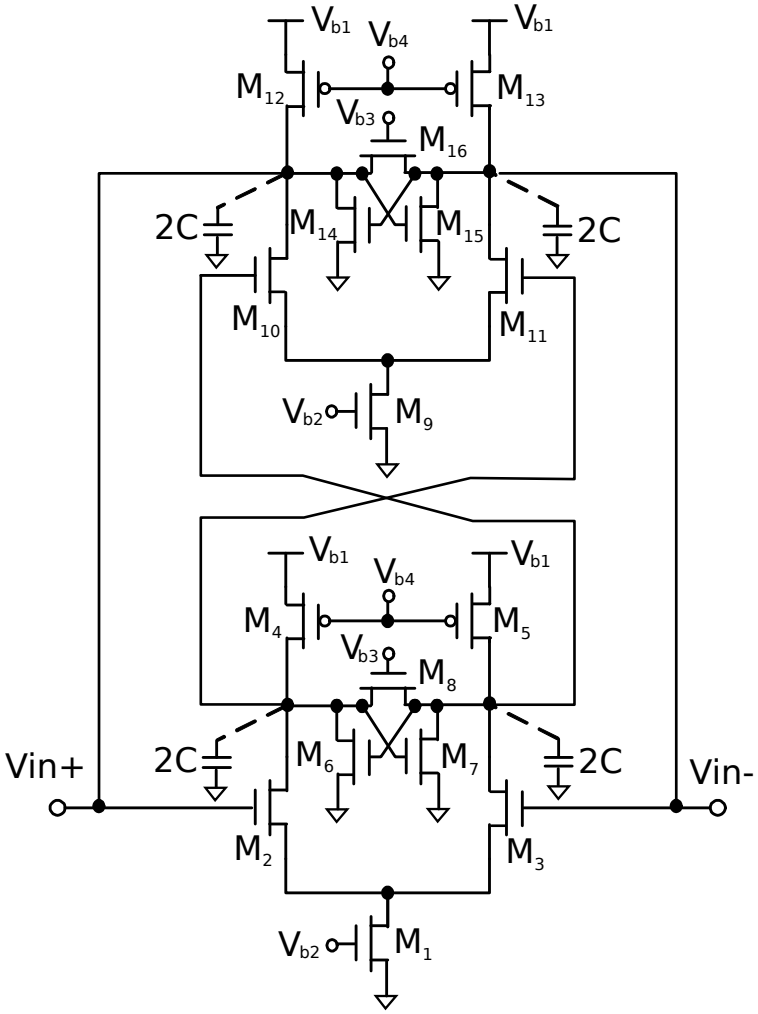


Figure 3.3: Simplified schematic of the Mahmoudi–Salama active inductor.

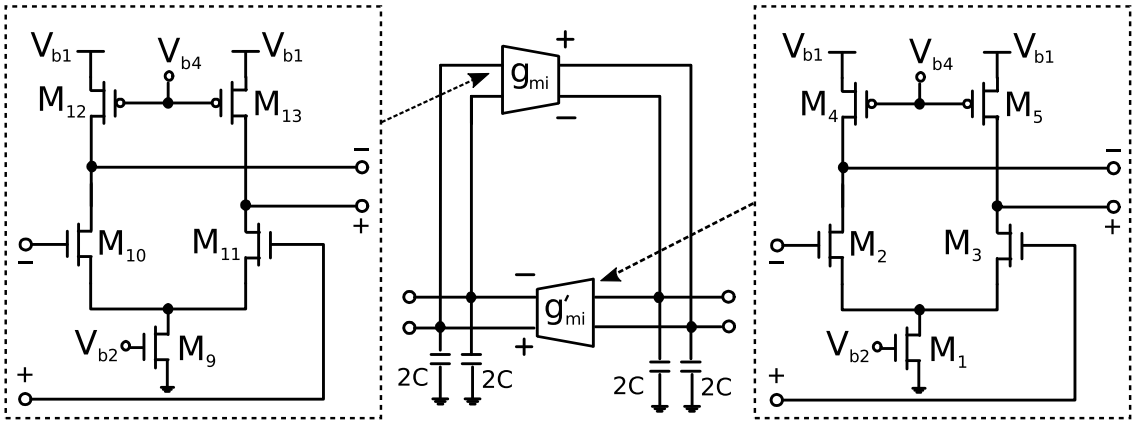


Figure 3.4: The principle diagram of the Mahmoudi–Salama differential active inductor.

Chapter 4
Design and Implementation of Analog Front-End

4.1 Selected Bandwidth Enhancement Technology for TIA Design

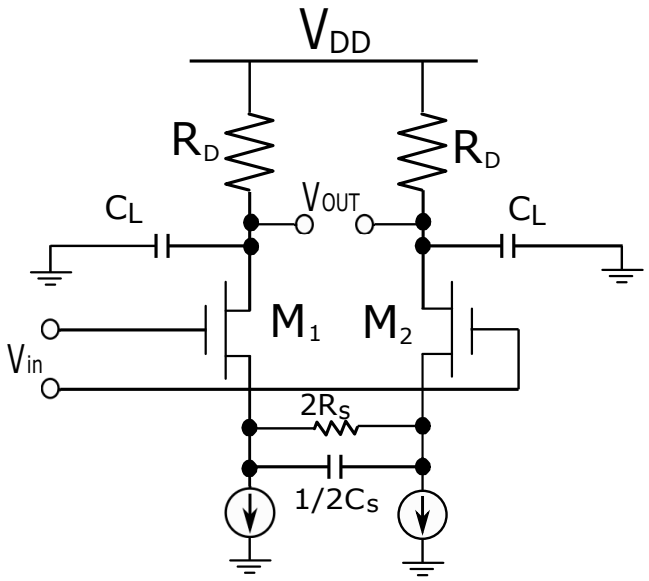
In the design of TIA, it is very important to choose the appropriate bandwidth enhancement technology. As described in Subsection 2.3, because the RGC topology has a very low input impedance and has a bandwidth advantage compared to CG-TIA, The author use RGC topology as the input stage of the TIA. Since the RGC structure has been described in detail in Subsection 2.3, it will not be repeated here. The following will introduce other traditional broadband technologies in detail.

4.1.1 Capacitive Degeneration

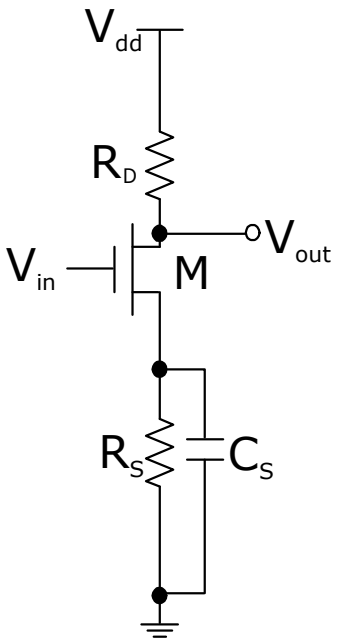
To produce a broadband response, it is possible to degenerate the transistors in a differential pair such that their effective transconductance increases at high frequencies. This compensates for the gain attenuation caused by the poles at the output nodes. Shown in Fig. 4.1(a), such an arrangement employs both capacitive and resistive degeneration.

As shown in Fig. 4.1(b), the voltage gain of a gain stage with capacitive degeneration is expressed by:

$$A_V = \frac{V_{out}}{V_{in}} = \frac{(g_{m1}R_D)(1+sR_SC_S)}{(1+g_{m1}R_S)(1+s\frac{R_SC_S}{1+g_{m1}R_S})}, \tag{4.1}$$



(a) Differential pair with capacitance degeneration



(b) Half-circuit equivalent

Figure 4.1: (a) Differential pair with capacitive degeneration, (b) Half-circuit equivalent.

which contributes a zero at $(R_S C_S)^{-1}$ and a pole at $\frac{1+g_{m1}R_S}{R_S C_S}$. The zero could be used to compensate the dominant pole of the circuit. The -3 dB cutoff frequency is therefore determined by the second lowest pole of the circuit [41].

4.1.2 Passive Broad-Band Matching Networks

The easiest way to increase the bandwidth of an existing amplifier topology is to increase the -3 dB cutoff frequency of each gain stage, which is usually achieved by reducing the corresponding resistive load. Smaller resistive loads mean lower gain and higher input-referred noise current. Because the gain and sensitivity of the front-end amplifier depend directly on the communication distance, it is desirable to maintain a constant gain while increasing the cutoff frequency. Passive matching networks could be used to explore the gain-bandwidth limitation without degrading other parameters of an existing amplifier [42]. The principle of increasing the gain-bandwidth product is to maintain a constant load over a wide frequency range. This can be achieved by a constant k filter, which means that the filter's passband gain is constant. The LC ladder filter in Figure 4.2 is such an implementation. According to the Bode-Fano limit, it has been proved that through a two-port passive matching network, the maximum gain bandwidth product that can be obtained can be increased up to four times. In other words, the bandwidth can be extended up to four times without changing the gain. Figure 4.2 shows the two port matching network, which is designed to exhibit nth-order Butterworth characteristic.

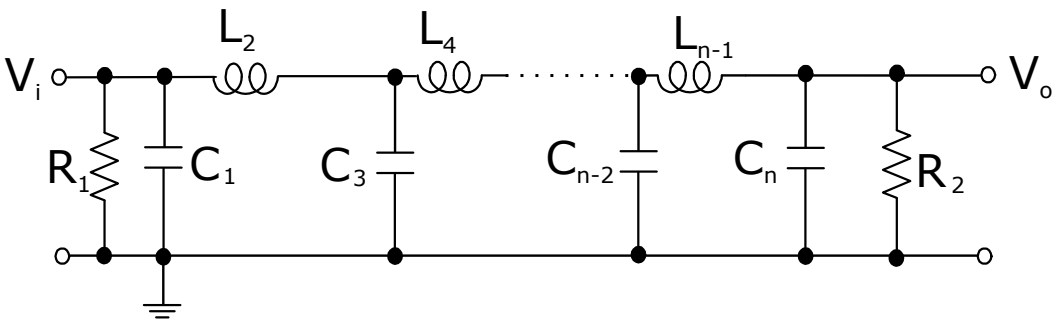


Figure 4.2: Small-signal model of an nth-order LC ladder filter.

4.1.3 A Conventional Transimpedance amplifier based on traditional broadband design technique

Figure 4.3 represents the schematic of a TIA based on the traditional broadband design technology. The TIA was composed of the following four parts: a matching network, an RGC input stage, a gain stage with capacitive degeneration, and a source follower output stage [41]. Figure 4.4 shows a chip microphotograph of the conventional TIA design. We can see that the spiral inductor takes up a large area of the chip, almost five times the area of the TIA core. Hence we have to explore ways to reduce the chip area to reduce costs.

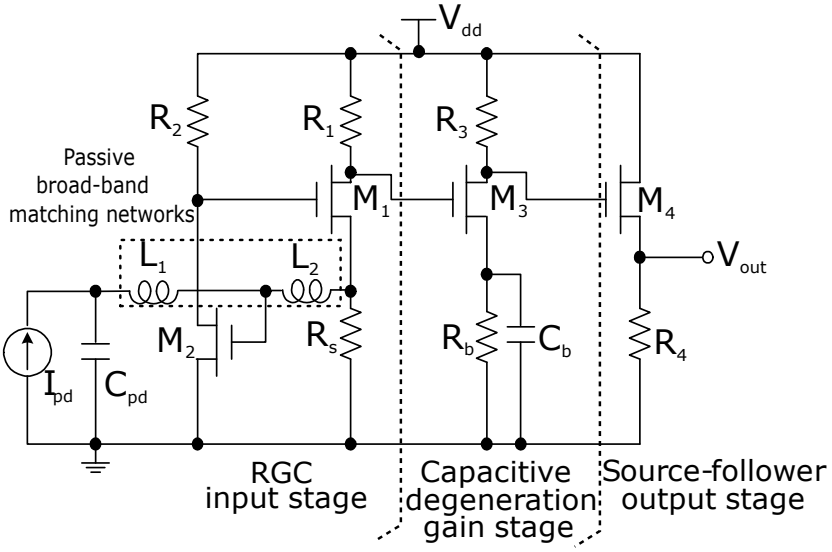


Figure 4.3: Schematic of a TIA based on traditional broadband design technology.

4.1.4 Frequency Characteristics of Mahmoudi-Salama Floating Active Inductor

In Chapter 3, the characteristics of floating active inductors are described in detail. When the parameters of a floating active inductor transistor are changed, its frequency characteristics change accordingly. Figure 4.5 shows the simulation results when the parameters of Mahmoudi-Salama FAI are shown in Table 4.1. We can see that the FAI had a good inductance characteristic when the frequency was within 100 GHz.

However, how exactly does the frequency characteristic change with changes in transistor parameters? Figure 4.6 shows the effect of the parameter values of M_8

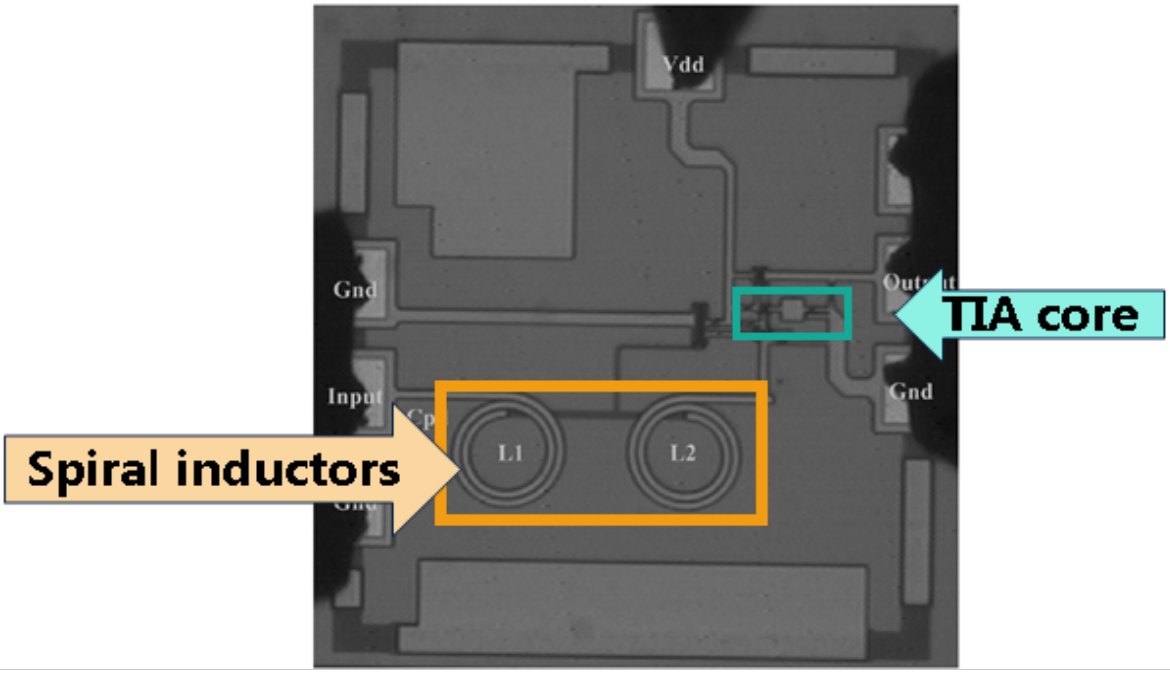


Figure 4.4: Chip microphotograph of the conventional TIA design [41].

Table 4.1: Device Parameters of floating active inductor in fig. 3.3

Parameters	
2C	100 fF
M_1, M_2, M_3, M_9, M_{10}, M_{11}	W/L=10 µm/0.18 µm, m=1
M_6, M_7, M_{14}, M_{15}	W/L=9 µm/0.18 µm, m=3
M_4, M_5, M_{12}, M_{13}	W/L=1.2 µm/0.5 µm, m=5
M_8, M_{16}	W/L=10 µm/0.18 µm, m=5
V_{b1}	1.5 V
V_{b2}	0.75 V
V_{b3}	1.8 V
V_{b4}	0 V

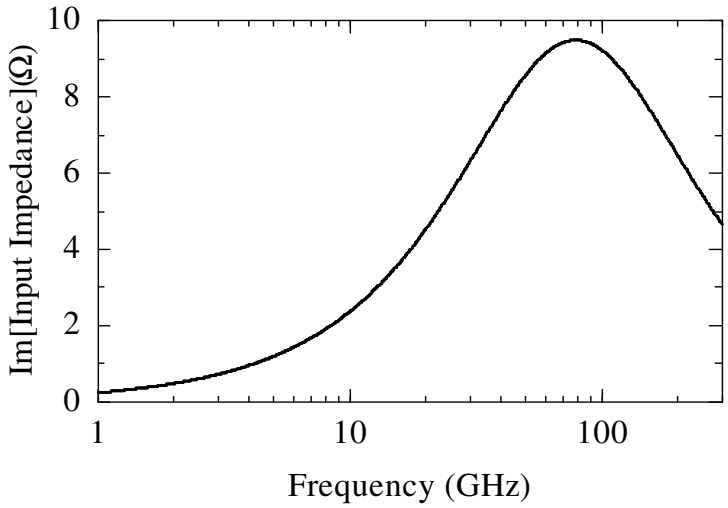


Figure 4.5: Frequency response of the Mahmoudi and Salama active inductor.

and M_{16} on the frequency characteristics of the FAI. As can be seen from Fig. 4.6, the parameter values of M_8 and M_{16} mainly affect the inductance value of the high frequency band of FAI. Figure 4.7 shows the effect of the parameter values of M_2 (M_3) and M_{10} (M_{11}) on the frequency characteristics of the FAI. It can be seen from Fig. 4.7 that M_2 (M_3) and M_{10} (M_{11}) mainly affects the movement of the peak of FAI, that is, the frequency range of working in an inductive state.

4.2 FAI-based TIA Design and Analysis

4.2.1 Proposed Circuit Topology

Figure 4.8 represents the schematic of a TIA based on FAI. The RGC input stage is well suited for broadband TIA design by its very low input impedance, compared with a single common-source follower and an inverter based amplifier. Thus, in this work, the proposed TIA is based on an RGC TIA. To reduce the chip area of TIA, an inductor L_2 was composed by an active inductor, which was named the Mahmoudi and Salama active inductor. Due to its good stability, the author chooses this type of active inductor (see Subsection 3.2).

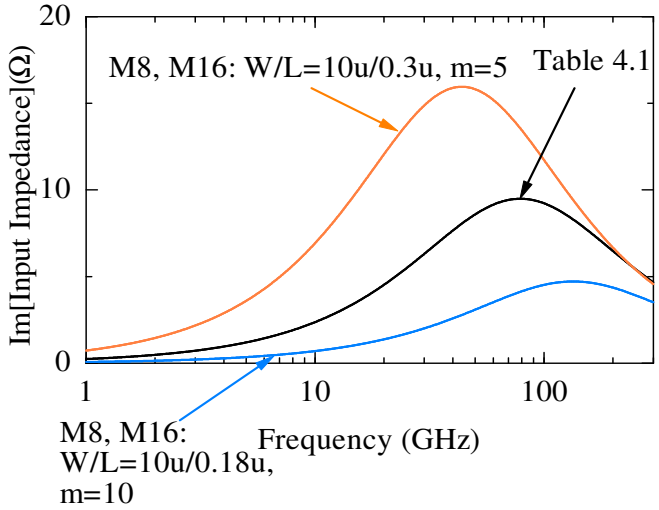


Figure 4.6: The effect of parameter values of M_8 and M_{16} on frequency characteristics.

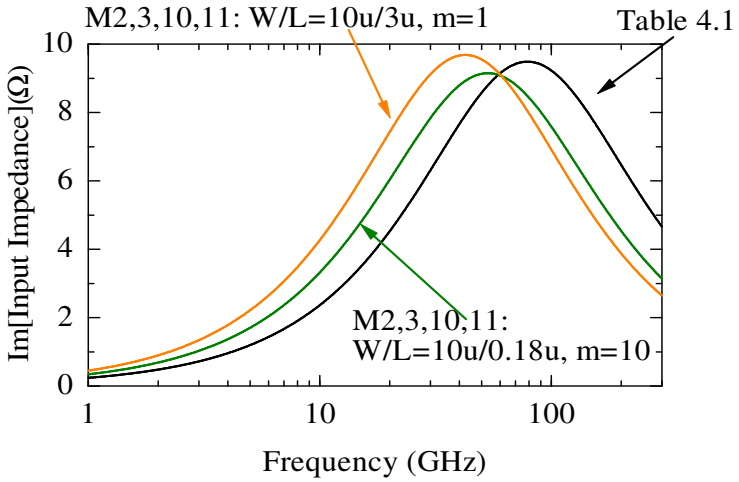


Figure 4.7: The effect of parameter values of M_2 (M_3) and M_{10} (M_{11}) on frequency characteristics.

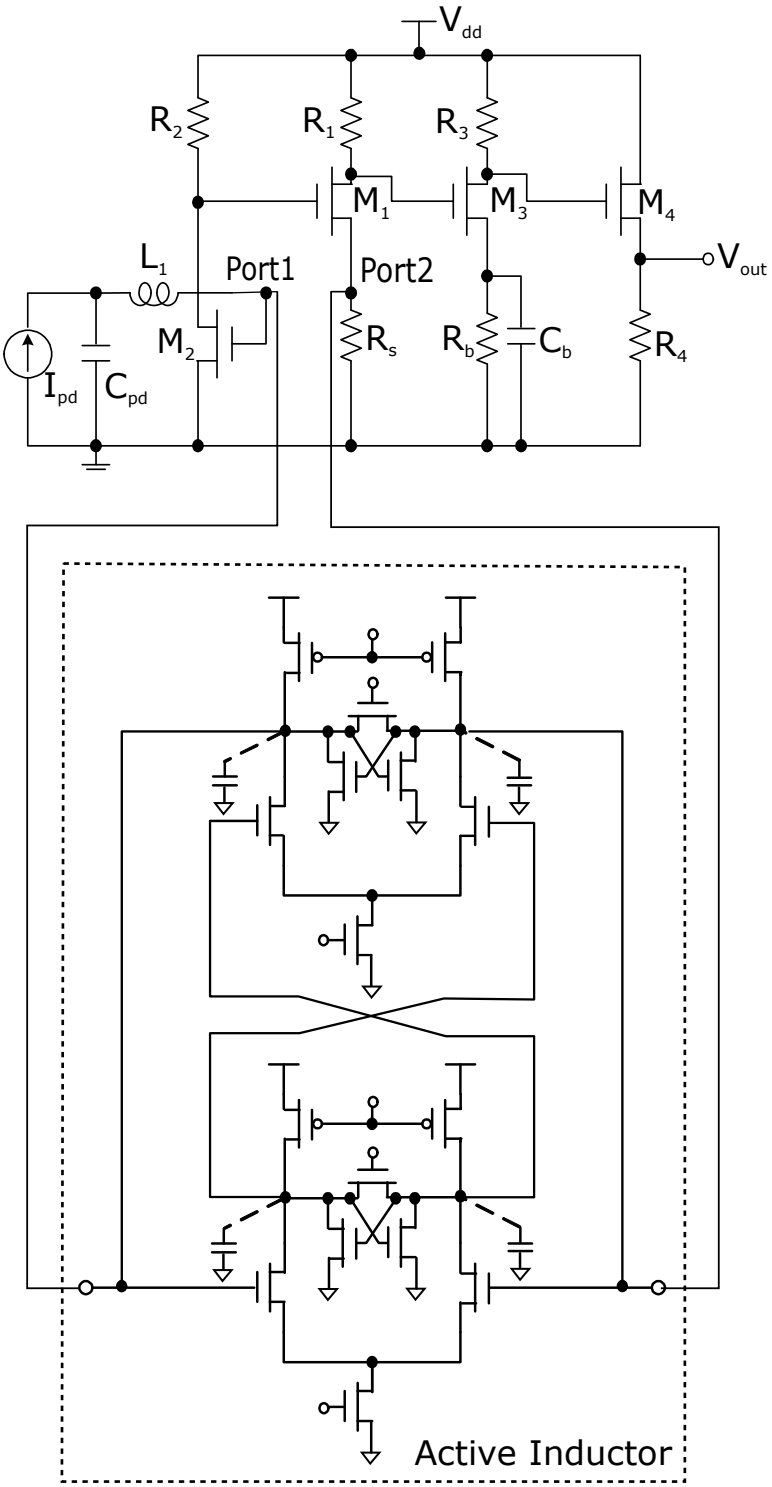


Figure 4.8: Schematic of the proposed TIA.

4.2.2 Proposed TIA Structure

The conventional TIA is shown in Fig. 4.3, where L_1 and L_2 are spiral inductors. In this work, the author change L_2 from spiral inductor to floating active inductor, i.e., Mahmoudi-Salama floating active inductor. As shown in Subsection 4.1.4, the values of the transistor parameters that make up FAI have a relatively large effect on the frequency characteristics of FAI. After simulation and analysis of FAI, the author selected a set of parameter values that can make FAI show stable inductive characteristics in 100GHz, as shown in Table 4.1. Unlike the conventional TIA in reference [41], the author assumes that L_1 is constructed by bonding wire in this work. It is well known that in general process, the inductance value of 1 mm bonding wire is between 2 nH and 2.5 nH. Therefore, the author uses the bonding wire as the inductor L_1, which is not on-chip, as shown in Fig. 4.8. In Subsection 4.3, the author will show the post-layout simulation results with the value of L_1 between 2 nH and 3 nH.

Because the input impedance of the RGC stage was very small, the lowest pole of the circuit was located within the TIA. In this TIA, a small R_2 was chosen to avoid possible peaking due to the zero generated by the local feedback of the RGC stage. Moreover, relatively large R_s is selected to minimize the noise current and signal loss. The capacitive degeneration gain stage consists of M_3, R_3, and R_b, and C_b contributed a zero $(R_bC_b)^{-1}$ that is used to compensate the lowest pole determined. M_4 and R_4 formed the source follower output stage which is used to drive the capacitance of the output pad.

The proposed TIA is also composed of four parts: a matching network implemented by FAI and bonding wire, the regulated cascode (RGC) input stage, the gain stage with capacitive degeneration and the source follower output stage.

4.2.3 Small Signal Analysis of RGC Stage in TIA

Figure 4.9 illustrates the small-signal model of the matching network and the RGC input stage. As described in Subsection 4.1.3, in the RGC stage of the proposed TIA, the author chooses a small R_2 to avoid possible peaking due to the zero generated by the local feedback of the RGC stage. Here, the author discusses the effects of inductors L_1, L_2 and R_s on proposed TIA through small signal analysis.

According to Kirchhoff's law, for each node in Fig. 4.9, we can write the following relationship:

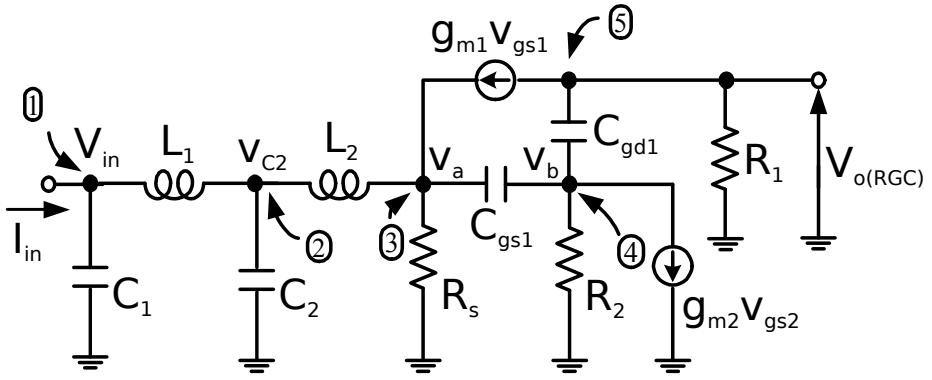


Figure 4.9: Small-signal model of the matching network and the RGC stage.

For Node 1,

$$-i_{in} + sC_1 v_{in} + \frac{1}{sL_1}(v_{in} - v_{c2}) = 0. \tag{4.2}$$

For Node 2,

$$-\frac{1}{sL_1}(v_{in} - v_{c2}) + sC_2 v_{c2} + \frac{1}{sL_2}(v_{c2} - v_a) = 0. \tag{4.3}$$

For Node 3,

$$-\frac{1}{sL_2}(v_{c2} - v_a) + \frac{1}{R_s}v_a + sC_{gs1}(v_a - v_b) - g_{m1}v_{gs1} = 0. \tag{4.4}$$

For Node 4,

$$-sC_{gs1}(v_a - v_b) + sC_{gd1}(v_b - v_{o,RGC}) + \frac{1}{R_2}v_b + g_{m2}v_{gs2} = 0. \tag{4.5}$$

For Node 5,

$$g_{m1}v_{gs1} - sC_{gd1}(v_b - v_{o,RGC}) + \frac{v_{o,RGC}}{R_1} = 0. \tag{4.6}$$

Here, g_{m1} and g_{m2} are the mutual conductance of the transistors M_1 and M_2 in RGC stage of the TIA shown in Fig. 4.3, respectively. C_1 is the parasitic capacitance of node 1, including photodiode capacitance $C_{\rm pd}$, and C_2 is the parasitic capacitance of node 2.

And we can write the equation of boundary conditions:

$$v_{gs1} = v_b - v_a, \tag{4.7}$$

$$v_{gs2} = v_{c2}, \tag{4.8}$$

$$v_{c2} = \frac{\frac{1}{sC_2}}{sL_1 + \frac{1}{sC_2}} v_{in}, \tag{4.9}$$

$$v_a = \frac{R_s}{sL_2 + R_s} v_{c2}, \tag{4.10}$$

$$v_b = \frac{R_2}{\frac{1}{sC_{gs1}} + R_2} v_a. \tag{4.11}$$

Here, from (4.2) and (4.11), the input impedance Z_{in} can be obtained as

$$Z_{in(s)} = \frac{v_{in}}{i_{in}} = \frac{sL_1(1 - C_2L_1)}{(1 - C_1L_1)(1 - C_2L_1) - 1}. \tag{4.12}$$

Also from Equations (4.3) to (4.11), we can obtain Eq. (4.13).

$$\left[\frac{1}{sL_1} - \frac{1}{1 - L_1C_2}\left(\frac{1}{sL_1} + sC_2 + g_{m2} + \frac{1}{sL_2R_S} + \frac{sR_sC_{gs1}}{1 + sR_2C_{gs1}}\right)\right] v_{in} = \frac{v_{o,RGC}}{R_1}. \tag{4.13}$$

From Equations (4.12) and (4.13), the expression of the transimpedance gain $Z_T(s)$ is obtained as shown in (4.14). In addition, we have the DC gain of the RGC as

shown in Equation (4.15).

$$\begin{aligned} Z_T(s) &= \frac{v_{o,RGC}}{i_{in}} \\ &= R_1 \left[\frac{1}{sL_1} - \frac{1}{1-L_1C_2} \left(\frac{1}{sL_1} + sC_2 + g_{m2} + \frac{1}{sL_2R_s} + \frac{sR_sC_{gs1}}{1+sR_2C_{gs1}} \right) \right] \\ &\times \frac{sL_1(1-L_1C_2)}{(1-L_1C_1)(1-L_1C_2)-1} \\ &= R_1 \left[1 - \frac{1}{1-L_1C_2} \left(1 - L_2C_2 + sg_{m2}L_1 + \frac{L_1}{L_2R_s} - \frac{R_sL_1C_{gs1}}{1+sR_2C_{gs1}} \right) \right] \\ &\times \frac{1-L_1C_2}{(1-L_1C_1)(1-L_1C_2)-1}. \end{aligned} \tag{4.14}$$

$$\begin{aligned} Z_T(s \to 0) &= R_1 \left[1 - \frac{1}{1-L_1C_2} \left(1 - L_2C_2 + \frac{L_1}{L_2R_s} - R_sL_1C_{gs1} \right) \right] \frac{1-L_1C_2}{(1-L_1C_1)(1-L_1C_2)-1} \\ &\approx R_1 \left[1 - \frac{1}{(1-L_1C_1)(1-L_1C_2)-1} \left(1 - L_2C_2 + \frac{L_1}{L_2R_s} - R_sL_1C_{gs1} \right) \right]. \end{aligned} \tag{4.15}$$

The original RGC gain was $Z_T(0)$, as shown in (4.15). In order to make the gain as large as possible, the term of $\frac{L_1}{L_2R_s}$ must be increased, that is the value of L_1 needs to be increased or the value of L_2R_s needs to be decreased. However, in this TIA, L_1 was the inductance of the bonding wire, which was almost fixed. As can be seen from Figure 4.5, the inductance of this FAI was very small. Therefore, we increased R_s above 500 Ω to increase the gain appropriately. Furthermore, a relatively large R_s could minimize noise current contribution and the signal loss due to it.

4.2.4 Noise Analysis

The TIA model with series inductive matching between the photodiode and the amplifier is renowned to be very helpful in reducing the frequency dependent noise and improving the front-end sensitivity [41, 43]. In [41], the equivalent input noise current spectral density of RGC TIA with inductor peaking was approximated as:

$$|i_{n,eq}|^2 = (1-\omega^2L_1C_{pd})^2I_n^2 + \omega^2C_{pd}^2E_n^2. \tag{4.16}$$

where C_{pd} stands for the photodiode parasitic capacitance. For a given $E_n - I_n$ noise model (see [41]), E_n and I_n are independent of the input matching network. Since L_1

is a negative term in (4.16), the noise reduction effect of L_1 can be clearly indicated. The effect of L_2 is similar to that of L_1. However, the effective inductance of L_2 is $L_{2,eff} = \frac{L_2}{(1+g_{m2}R_2)}$, which is relatively small; hence, the noise reduction effect of L_2 should be less than that of L_1 [41]. Consequently, we can come to the conclusion that increasing the effective value of the inductor in this topology could reduce the input referred noise, in theory.

Figure 4.10 shows the comparison of input-referred noise current spectral density of TIA with FAI and TIA with spiral inductor. This pre-layout simulation results are performed in Spice simulator under the same simulation conditions. Since the pre-layout simulation results do not include the influence of parasitic capacitance and other factors, the noise performance is better than that of the post-layout simulation results. It is well known that the noise performance of FAI is worse than spiral inductor. This can also be seen from the simulation results in Fig. 4.10. However, from Figure 4.10, we can see that the input-referred noise current of the TIA with the spiral inductor is 11.01 pA/$\sqrt{\text{Hz}}$, and the input-referred noise current of the TIA with the active inductor is 13.48 pA/$\sqrt{\text{Hz}}$, that is, the input-referred noise of the two TIAs differ by only 2.47 pA/$\sqrt{\text{Hz}}$. Therefore, we can infer that the shortcomings of larger input-referred noise current caused by FAI can be ignored.

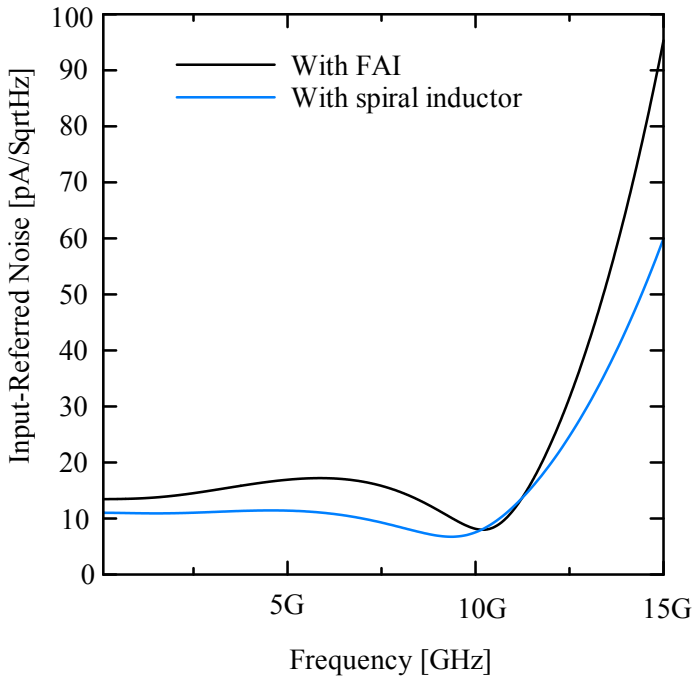


Figure 4.10: Input-referred noise current spectral density of TIA with FAI and with spiral inductor.

4.3 Implementation and post-layout Simulation Results of Proposed TIA

To evaluate the performance of the proposed TIA, it is implemented using 0.18 µm Rohm CMOS technology. All post-layout simulation results are performed in Cadence.

The layout of the top cell with the pad and TIA core is shown in Figs. 4.11 and 4.12, respectively. Correspondingly, they occupied layout areas of 1590 µm × 780 µm and 180 µm × 118 µm. Figure 4.13 shows the chip microphotograph of the proposed TIA.

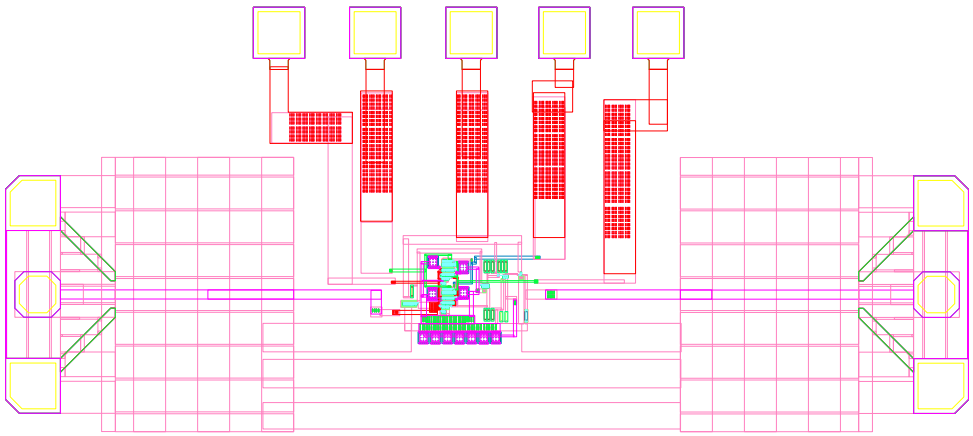


Figure 4.11: Layout of the proposed TIA (top cell with pad).

Figure 4.14 shows the pre-layout simulation results of the frequency characteristics, and the −3 dB bandwidth was 16 GHz. Figure 4.15 shows the post-layout frequency response of the proposed TIA. We can see from the simulation results that no matter what value L_1 took between 2 nH and 3 nH, the transimpedance gain was about 41 dBΩ, and the −3 dB bandwidth was greater than 10 GHz in the presence of a C_{pd} of 150 fF. The conclusion was that any value between 2 nH and 3 nH of the bonding wire worked well with this design and gave good frequency characteristics. By comparing Fig. 4.15 and Fig. 4.14, it can be seen that the −3 dB bandwidth of post-layout simulation is reduced by approximately 6 GHz compared to the −3 dB bandwidth of pre-layout simulation.

In this post-layout simulation, the PRBS generator is implemented using linear feed back shift registers (LFSR). Figure 4.16 shows an input signal at the rate of 15 Gb/s from an implemented LFSR. These PRBS outputs had a jitter of 2 ps. Figure 4.17 shows the eye-diagram for the input signal currents of 100 μA_{pp}

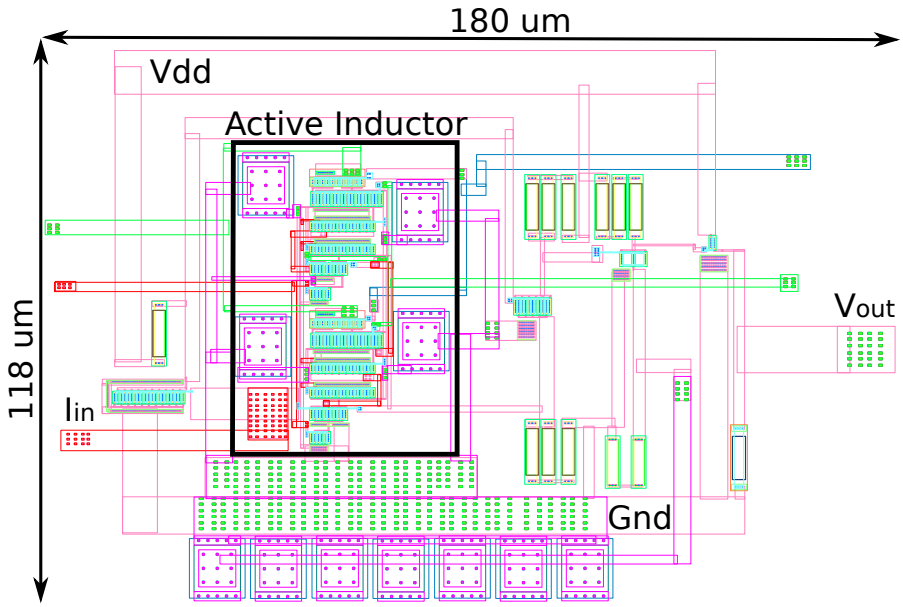


Figure 4.12: Layout of the proposed TIA (TIA core).

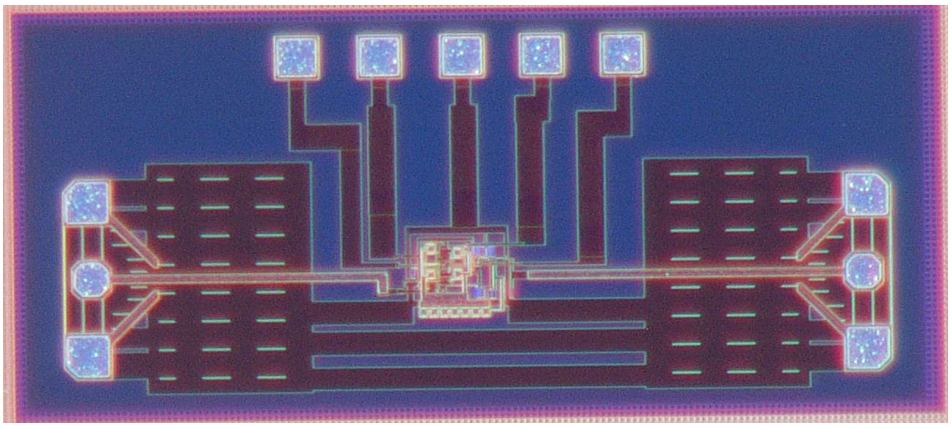


Figure 4.13: Chip microphotograph of the proposed TIA design.

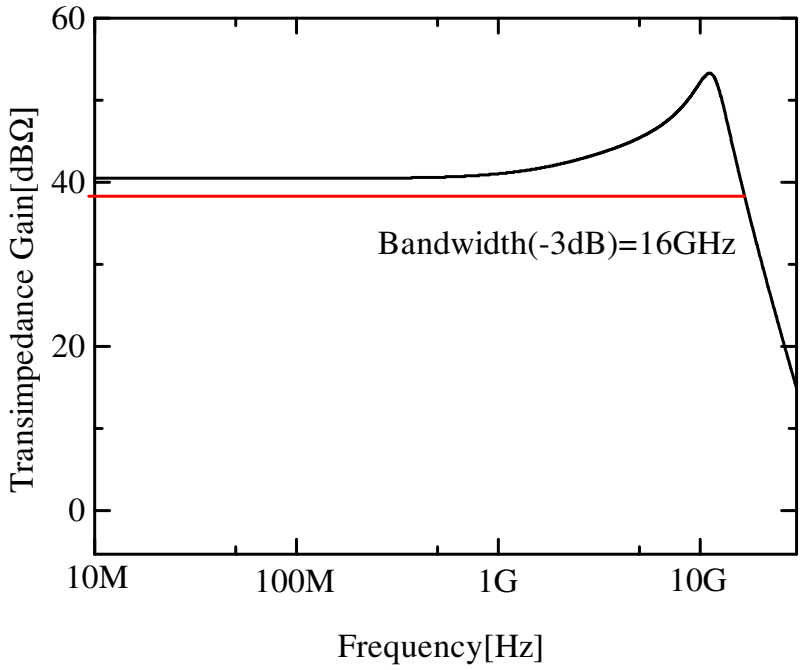


Figure 4.14: Pre-layout simulated frequency response of the proposed TIA.

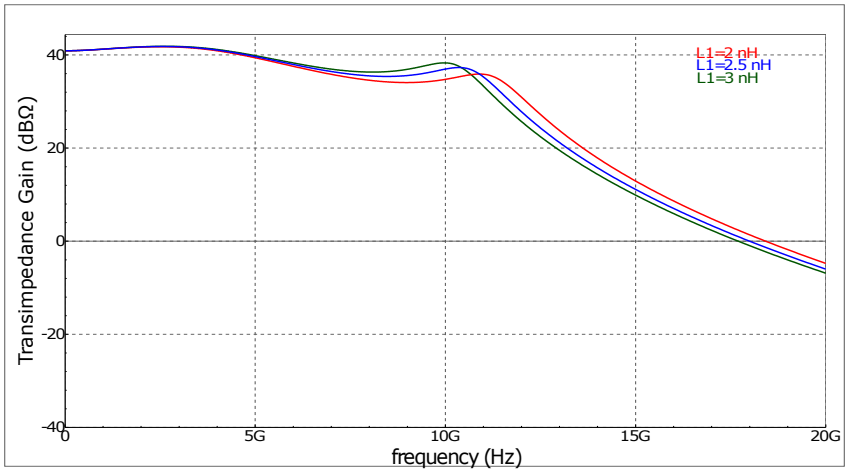


Figure 4.15: Post-layout simulated frequency response of the proposed TIA.

$2^{31} - 1$ pseudo-random bit sequence (PRBS) at the rates of 5 Gb/s, 10 Gb/s, and 15 Gb/s. From the post-layout simulation results, the proposed TIA could generate the waveform with good eye-opening owing to the wide bandwidth. The jitter of the post-layout simulation was 4.03 ps when the bit rate was 15 Gb/s. Table 4.2

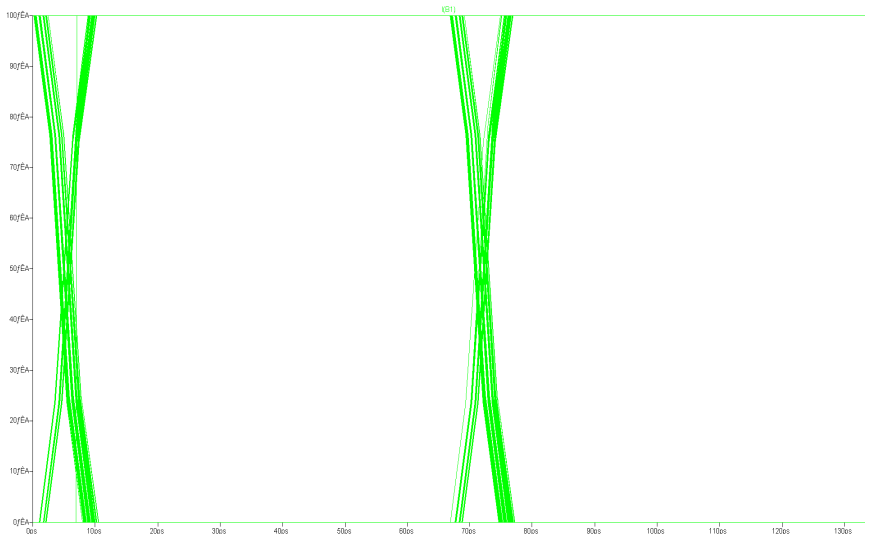


Figure 4.16: input signal with a jitter.

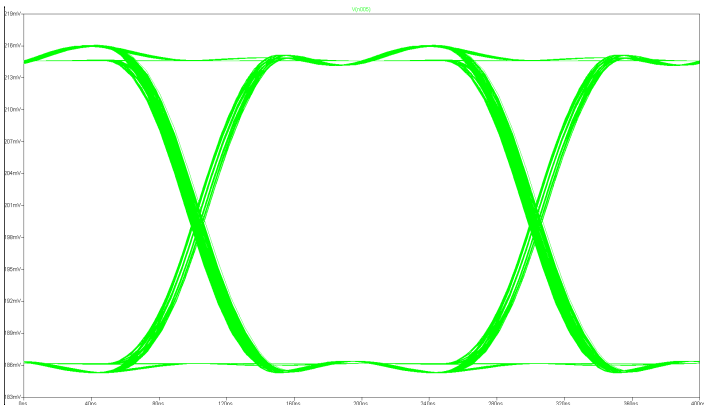
compares the performance of the proposed TIA with other recently published TIAs. It can be clearly seen that the presented work was superior in terms of bandwidth, power dissipation, and chip area compared with other TIAs implemented using the same 0.18 µm CMOS technology.

The standard figure of merit (FoM) is calculated as (4.17) below and is used to compare this design with other recent TIA designs in Table 4.2.

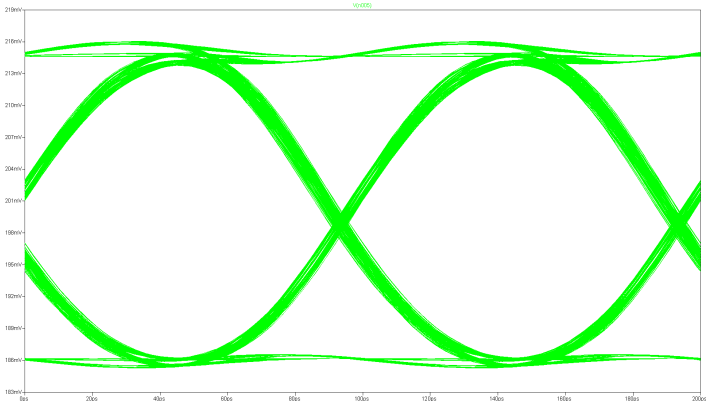
$$\text{FoM} = \frac{\text{Gain(dB}\Omega) \times \text{Bandwidth(GHz)} \times \text{C}_{\text{pd}}\text{(pF)}}{\text{Power(mW)} \times \text{Chip Area (mm}^2\text{)}} \tag{4.17}$$

It can be seen that this design was better in terms of FoM compared with the conventional design using the same process. The input referred noise of the proposed TIA was increased by a factor of approximately 1.7, compared with the conventional TIA. The main cause of the increase of input referred noise was that the effective value of the active inductor we used was much smaller than the effective value of the spiral inductor in the conventional TIA. Furthermore, we assumed that the bonding wire L_1 was 2 nH to connect the photo-diode (PD). However, in the conventional TIA, the spiral inductor of L_1 was 0.77 nH, which was not including the inductance of PD connection. The actual value of L_1 in the conventional TIA could be approx-

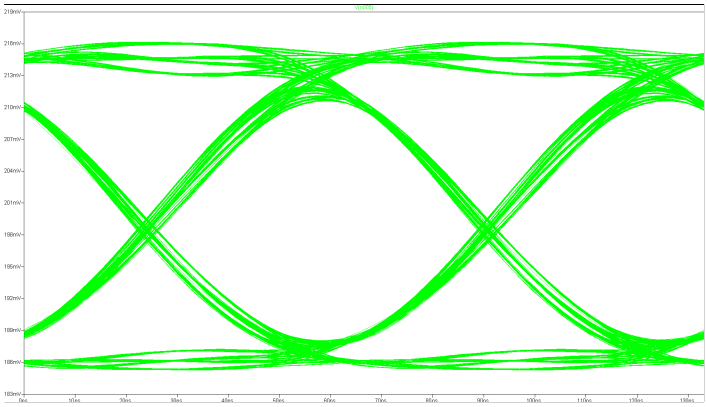
imately expressed as $L_1(\text{Actual}) = \text{L}_1 + \text{L}(\text{PD}_{\text{Connection}})$. In other words, assuming that the inductance of the bonding wire was the same, the effective value of L_1 of the conventional TIA was actually 0.77 nH larger than that of the proposed TIA. This also increased the input referred noise to a considerable extent. Nevertheless, the noise performance of the proposed TIA was also better than that of the general TIA without a matching network of inductors.



(a) Bit-rate: 5 Gb/s



(b) Bit-rate: 10 Gb/s



(c) Bit-rate: 15 Gb/s

Figure 4.17: Eye-diagram characteristics with a $2^{31}-1$ pseudo-random bit sequence (PRBS) input current of 100 μA_{pp} at (**a**) 5 Gb/s, (**b**) 10 Gb/s, and (**c**) 15 Gb/s.

Table 4.2: Performance summary and comparison with other works

Reference	[41]	[17]	[15]
Technology	180 nm CMOS	180 nm CMOS	180 nm CMOS
Topology	RGC+Inductor Peaking	RGC+Inductor Peaking	CS+Inductor Peaking
Supply Voltage	1.8 V	1.8 V	1.8 V
Transimpedance Gain (dBΩ)	53	55	51
Bandwidth (GHz)	8	7	30.5
C_{pd} (fF)	250	200	50
Power Dissipation (mW)	13.5	18.6	60.1
Input-Referred Noise (pA/$\sqrt{\text{Hz}}$)	18	17.5	55.7
Chip Area (μm^2)	450 × 250	400 × 250	1170 × 460
FoM	70.75	41.4	2.4
Results	Measured	Measured	Measured
	[21]	**[16]**	**[11]**
	180 nm CMOS	180 nm CMOS	80 nm CMOS
	CS+NI+AI	RGC+AI	CG+Inductor Peaking
	1.8 V	1.8 V	1 V
	54.3	56	52
	7	8.27	20
	50	300	100
	29	35	2.2
	5.9	20	50
	230 × 45	106 × 100	140 × 70 (*49613 μm^2)
	63.3	360.6	952.8
	SPICE	Post-layout	Measured
	[18]	**[7]**	**This work**
	40 nm CMOS	28 nm CMOS	180 nm CMOS
	Inverter+CD	CG+AI	RGC+AI
	1.1 V	1 V	1.8 V
	47	43	41
	8	22	10
	250	150	150
	2	2	10.7
	23	N/A	30.7
	200 μm^2 (*4050 μm^2)	18 × 23 (*17110 μm^2)	180 × 118
	11604.75	4146.6	270.6
	Post-layout	Measured	Post-layout

CS: Common Source, NI: Negative Impedance, AI: Active Inductor, CG: Common Gate, CD: Common Drain, *Scaled Chip Area by $Area(scaled) = Area(actual) \times (\frac{180(nm)}{Process(nm)})^2$

4.4 Design of Lmiting Amplifier (LA)

Differential versions of Cherry-Hooper amplifiers used in limiting amplifier often take the configuration shown in Fig. 4.18 (**a**). Since PMOS or pnp current source typically contribute substantial capacitance to the output nodes [34], I_1 and I_2 are replaced by resistors as shown in Fig. 4.18 (**b**). And to alleviate the gain headroom trade-off, the circuit can be modified are shown in Fig. 4.19.

Figure 4.20 depicts a schematic diagram of the proposed analog front-end network. In order to use a the Cherry-Hooper differential amplifier, a replica TIA is added. In this design, an unbalanced pseudo-differential TIA with one photodetector is used, as shown in Fig. 4.20. This part consists of a single-ended main TIA and a matching replica TIA (a.k.a dummy TIA). The replica TIA simply produces a DC voltage that tracks the dark level of the voltage over process, voltage and temperature. To alleviate the gain-headroom trade-off, we use the modified Cherry-Hooper amplifier, where the resistors provide part or all of the bias current of the input differential pair. In this LA, R_H must be much greater than the input resistance of the second stage to avoid degarding the gain. In order to achieve the matching with the subsequent circuits and achieve the maximum power output, the LA must use the output buffer unit to achieve output impedance matching and improve the driving capability of the circuit.

We have completed the overall design of the LA and are currently simulating the LA. The simulation results so far are shown in the appendix.

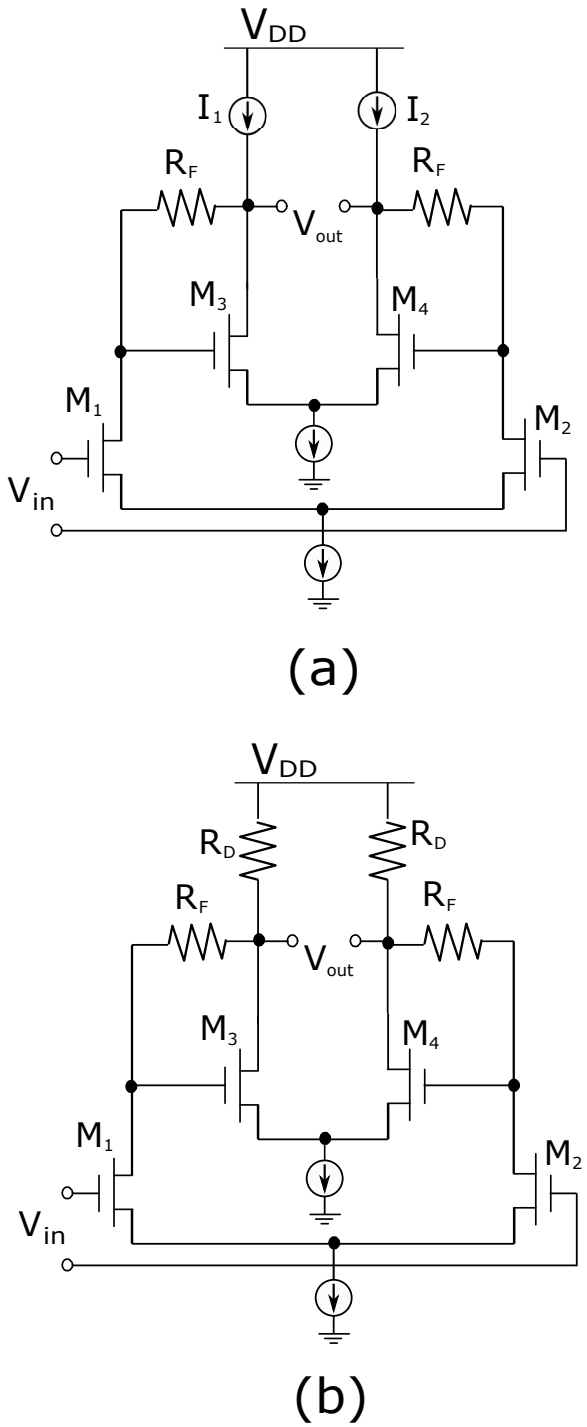


Figure 4.18: Differential Cherry-Hooper amplifier with (**a**) current-source loads and (**b**) resistive loads.

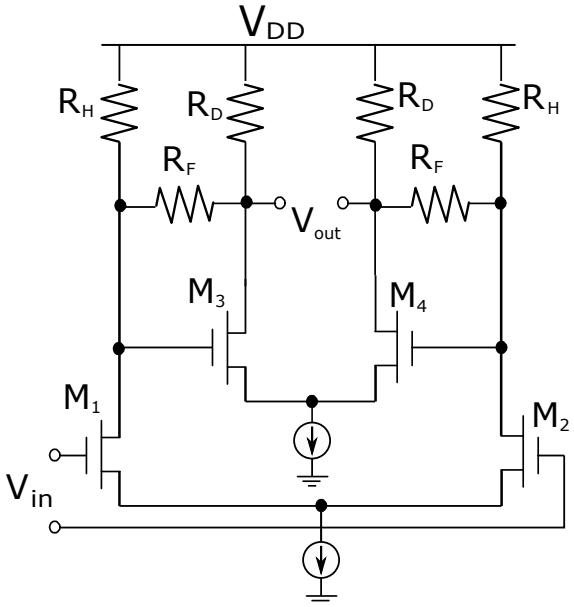


Figure 4.19: Modified Cherry-Hooper amplifier.

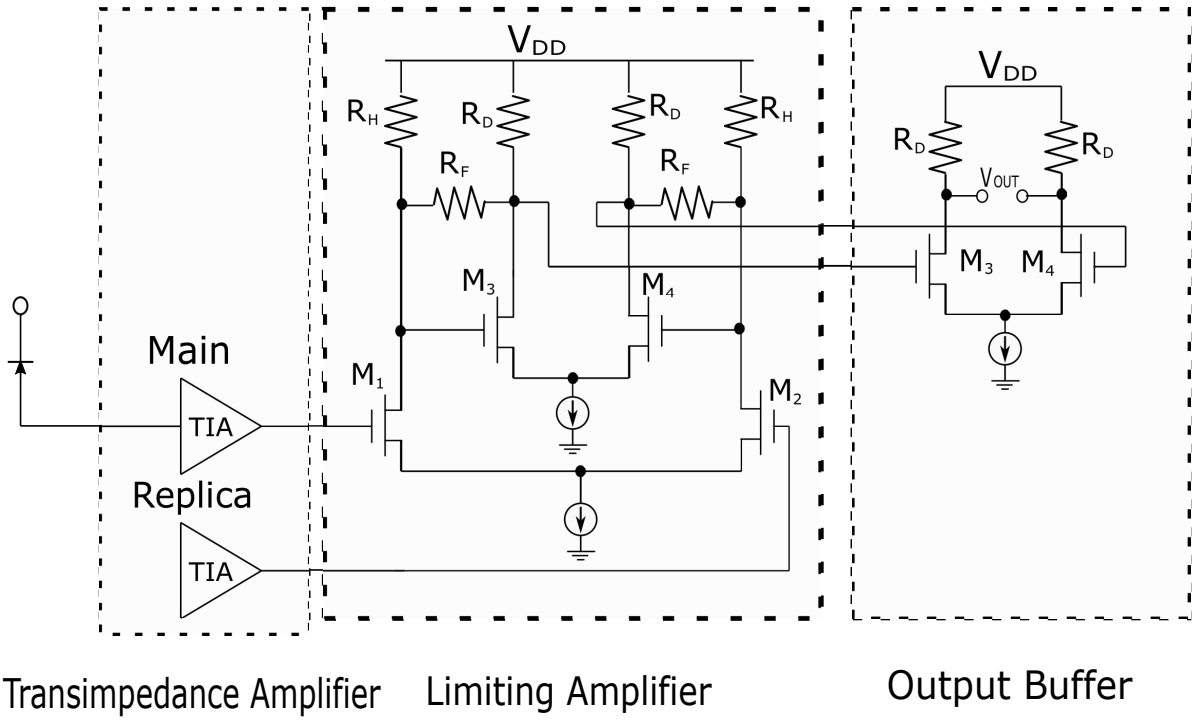


Figure 4.20: Schematic of the proposed analog front-end.

Chapter 5

Conclusions and Future Works

5.1 Conclusions

In this work, a 15 Gb/s optical receiver trans-impedance amplifier (TIA) based on floating active inductor (FAI) for 10G-PON deployments has been designed and implemented using a 0.18 μm CMOS process. The proposed TIA exhibits the following characteristics: a −3 dB bandwidth greater than 10 GHz and a transimpedance gain of 41 dBΩ. Owing to the use of FAI, the area of the chip was greatly reduced and was almost 18.8% of that of the conventional TIA. Moreover, because the parameters and resistance value of the transistor were different from the conventional TIA, the simulation results showed that the floating active inductor did not increase the power dissipation. In contrast, the proposed TIA had a lower power dissipation of 10.7 mW. Thus, the post-layout simulation results indicated that the floating active inductor was very useful in optical applications.

In order to increase the gain of the proposed TIA so that the output voltage can meet the requirements of the decision circuit, the author also designed the LA that follows the TIA. The proposed analog receiver front-end circuit contains an unbalanced psedudo-differential TIA with floating active inductor, a LA of modified Cherry-Hooper amplifier, and a differential output buffer stage. The proposed AFE circuit achieves −3 dB frequency of 10 GHz and gain of 70 dBΩ.

5.2 Future Works

The TIA results presented in this dissertation are all post-layout simulation results. Because the chip has been successfully taped out, the author next will actually test the chip and compare it with the post-layout simulation results. In addition, for the

subsequent cascaded LA circuit of the designed TIA, although its bandwidth and gain performance is good, it still stays at the bit rate of 5 Gb/s. So the next step is to continue to improve it. After increasing the transmission rate of LA to above 15 Gb/s, the author's next plan is layout and tape out for the proposed analog front-end circuit , and finally test the chip of the analog front-end circuit.

Appendix A
Simulation Results of PA

Figure A.1 and Figure A.2 show the frequency characteristics and eye diagram of proposed AFE circuit, respectively. The eye-diagram is for the input signal currents of 100 μA_{pp} $2^{15} - 1$ pseudo-random bit sequence (PRBS) at the rates of 5 Gb/s. The proposed AFE circuit achieves -3 dB frequency of 10 GHz and gain of 70 dBΩ. Currently, LA exhibits good bandwidth and gain characteristics. However, from the current simulation results, the eye-opening of LA is not completely satisfactory. So finding the parameters suitable for AFE circuit is also the author's next work. The main improvement idea is to reduce the gain appropriately to obtain a higher transmission rate when the gain and rate cannot be met at the same time.

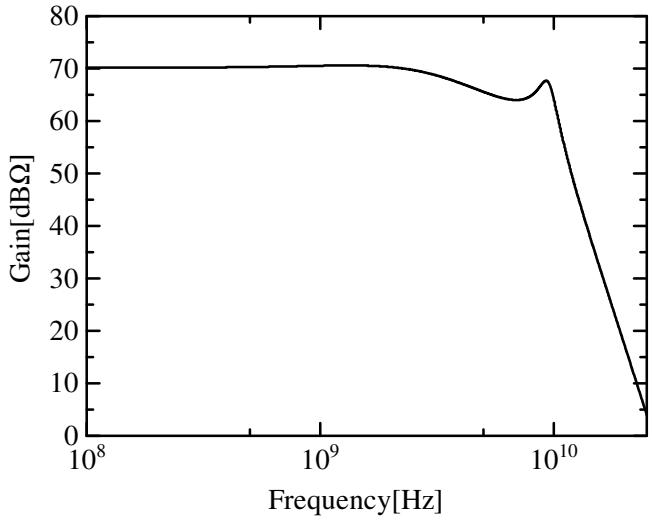


Figure A.1: Frequency response of the proposed analog front-end..

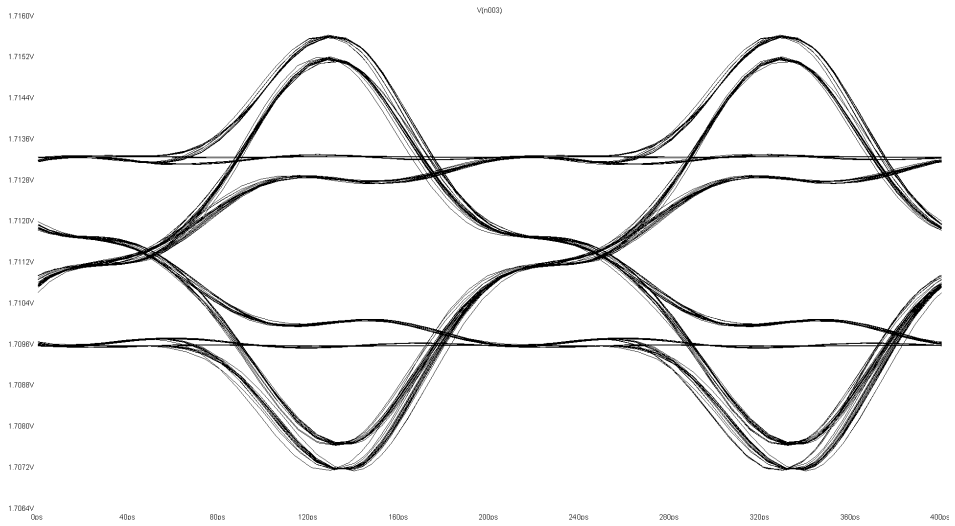


Figure A.2: Eye diagram of proposed LA.

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