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# Overlapped-voltage clock driver and low peak voltage evaluation for 2PASCL

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## Abstract

The paper proposes the best conditions for the power supply clocks of two-phase clocked adiabatic static CMOS logic (2PASCL) circuit by evaluating several overlapped clock combinations and measure the power dissipations using SPICE simulation. Then, the reduced peak driving voltage of 1.2 V for 2PASCL and CMOS are compared.

## 1 Introduction

The low-power 2PASCL [1] circuit uses two complementary split-level sinusoidal power supply clocks,  $V\phi$  and  $V\bar{\phi}$  whose height is equal to  $V_{dd}$ . From the simulation results, we find that 2PASCL 4-inverter chain logic can save up to 79% of dissipated energy as compared to that with a static CMOS logic at transition frequencies of 1 to 100 MHz. In this paper, we evaluate the overlapped power supply clocks to further reduce its power dissipation. Then, with 4-inverter chain as test vehicle, we simulate the peak voltage of 1.2 V using 0.18  $\mu\text{m}$  standard CMOS process SPICE simulation, and compared the results with CMOS.

## 2 Best conditions of 2PASCL to reduce power dissipation

### 2.1 Overlapped power clocks

Figure 1 demonstrates the 2PASCL circuit where  $X$  is the input and  $V_j$  is the output. As shown on the second graph of the output waveforms, split-level sinusoidal clocks are used to drive the circuit.

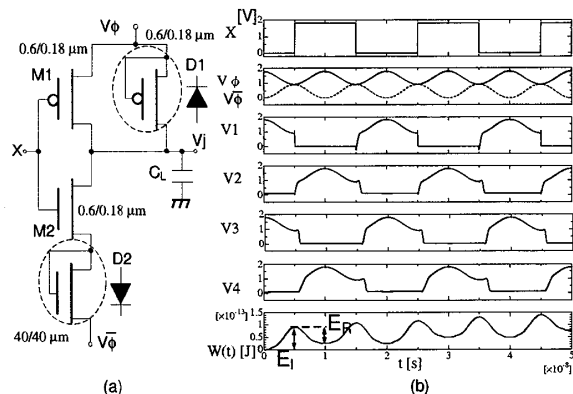


Fig. 1 (a) 2PASCL circuit, and (b) its 4-inverter chain output waveforms.  $V_1$ ,  $V_2$ ,  $V_3$ , and  $V_4$  is the output voltage at each inverter. Energy dissipation at each transition =  $E_I$ (injected energy) -  $E_R$ (received energy).

By taking “0” as the voltage point of 0.9 V; for the minimum voltage of  $V\phi$  and maximum voltage of  $V\bar{\phi}$ , we evaluate the “-” values where those clocks are separated and “+” values where they are overlapped. From the power dissipation result per cycle from the simula-

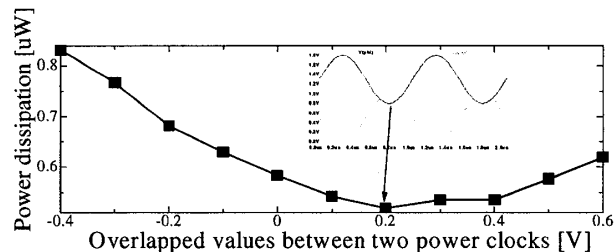


Fig. 2 Supply clocks combinations and the power dissipations.

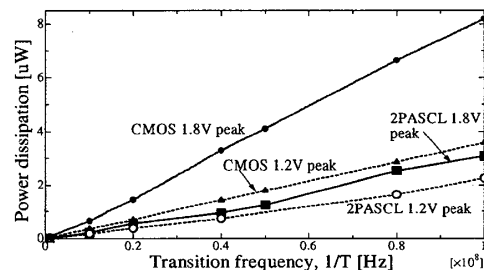


Fig. 3 Power dissipation of 4-inverter chain of 2PASCL and CMOS logics at different peak voltage.

tion as shown in Fig. 2, we understand that with the gap of 0.2 V overlapped between each clocks, it shows the lowest in energy dissipation.

### 2.2 Low peak voltage clock evaluation

From earlier simulation, the threshold voltage of nMOS,  $V_{tn}$  is 0.58 V and for pMOS,  $V_{tp}$  is -0.24 V. By reducing the peak voltage of the power clock we compared the power dissipation of CMOS and 2PASCL. This evaluation is to find the minimum operating voltage clock with 0.18  $\mu\text{m}$  process to drive a 4-inverter chain accordingly. The results are as shown in Fig. 3.

From the results, to drive the circuit at 1.2 V is feasible. The power dissipation of 1.8V 2PASCL peak voltage is lower than that of 1.2 V CMOS  $V_{dd}$ .

## Conclusion

By introducing the gap of 0.2 V of overlapped power clock voltage, about 10% of energy can be saved as compared with non-overlapping voltages. Furthermore, 4-inverter chain of 2PASCL can be operated at minimum 1.2 V and reduces up to 65% as compared to that with CMOS operated at 1.2 V  $V_{dd}$ .

## Reference

- [1] N. Anuar, Y. Takahashi and T. Sekine, “Adiabatic logic versus CMOS for low power applications,” *Proc. ITC-CSCC 2009*, pp.302–305, Jul. 2009.